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ABSTRACT

These volumes are, respectively, the self-instructional student manual and the teacher manual that cover the third set of training topics in this course for television repair technicians. Both contain identical information on synchronization and deflection circuits, including sections on the principle of synchronized deflection, synchronization circuits, vertical deflection circuits (VDCs), horizontal deflection circuits (HDCs), surrounding circuits of the horizontal deflection circuits, and pincushion circuits. Functional block diagrams and circuit diagrams are included. (CML)

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TV TROUBLE-SHOOTING MANUAL
VOLUMES 7-8

Part 3: Synchronisation and Deflection Circuits

Student and Instructor's Manuals

Asian and Pacific Skill Development Programme
Islamabad, Pakistan

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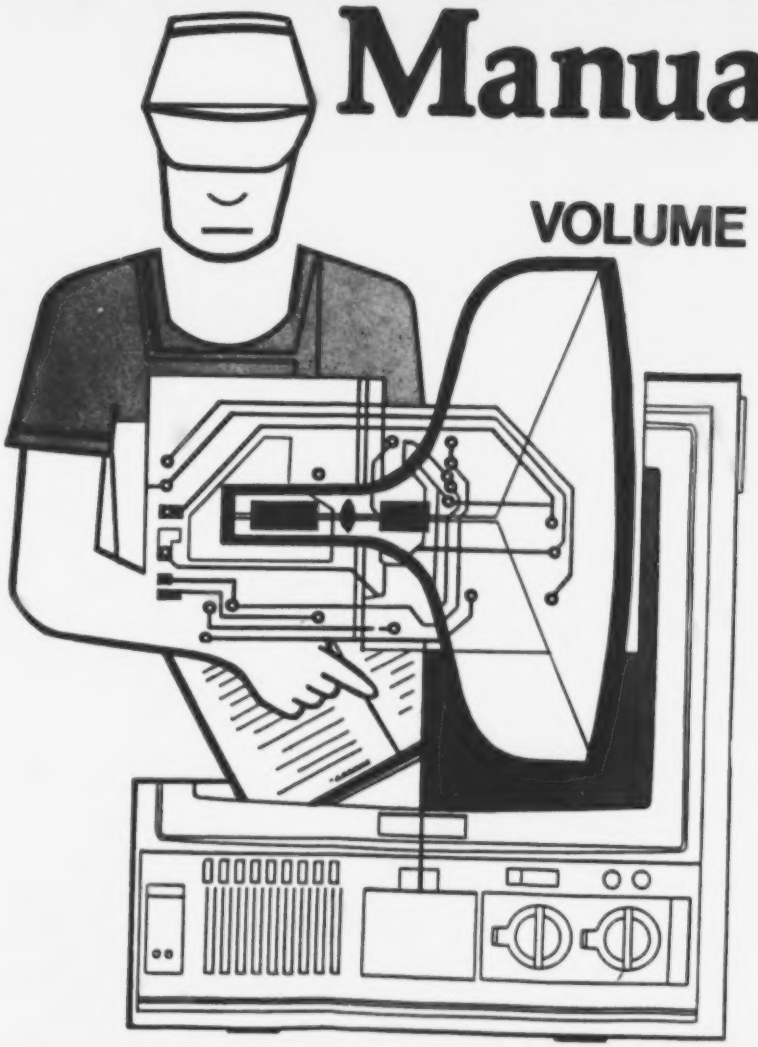
TV Trouble-shooting Manual

VOLUME



BY MASAAKI MUKAI AND RYOZO KOBAYASHI

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TV Trouble-shooting Manual

VOLUME 7

BY MASAAKI MUKAI AND RYOZO KOBAYASHI

Part 3: Synchronisation and deflection circuits

ASIAN AND PACIFIC SKILL DEVELOPMENT PROGRAMME
INTERNATIONAL LABOUR OFFICE
ISLAMABAD, PAKISTAN, 1988

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Part 3: Synchronisation and deflection circuits

Principle of synchronised deflection

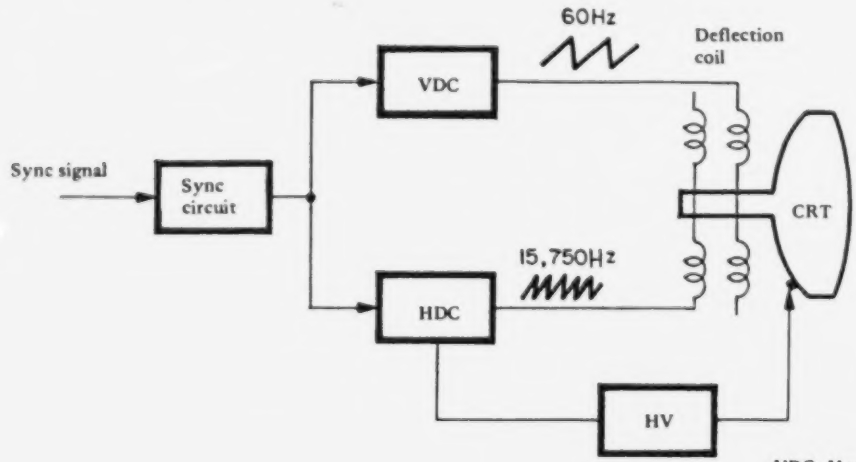
The deflection of the modulated electron beam must be synchronised with the image to be reproduced. The beam must be deflected in successive order from left to right and from top to bottom. The deflection must be timed so that the picture elements are assembled in the same way the camera at the transmitter disassembles the image to be transmitted.

The timing of the beam's horizontal and vertical deflection is called synchronisation. There are two methods of deflection: static and electromagnetic. Permanent magnets are used in static deflection, electromagnetic coils in electromagnetic deflection. Electromagnetic deflection is used in TV receivers.

Sawtooth currents are supplied to the deflection coils to produce an electromagnetic field needed to deflect an electron beam. The frequencies of the currents for horizontal and vertical deflection coils are 15,750 Hz and 60 Hz, respectively.

The deflection of the electron beam or the scanning of the cathode-ray tube (CRT) is synchronised with the scanning of the camera at the transmitter by sync signals transmitted with the video signal.

Figure 3-1 shows a block diagram of the deflection circuits.



VDC: Vertical deflection circuit
HDC: Horizontal deflection circuit
HV: High voltage

Figure 3-1
Functional block diagram of synchronisation and deflection circuits

Electron beam deflection

Figure 3-2 illustrates the principle of static deflection. The magnitude and direction of the beam's deflection depend on the strength and direction of the magnetic field.

The direction of the beam can be determined using Flemming's left-hand rule (see Figure 3-3). Examples of the direction of the beam's deflection and the corresponding direction of the magnetic fields are shown in Figure 3-2.

CRTs in television receivers use a pair of coils for deflecting the electron beam. These are the horizontal and vertical deflection coils. Each sawtooth current flowing through the coils produces varying electromagnetic fields, which deflect the beam all over the screen.

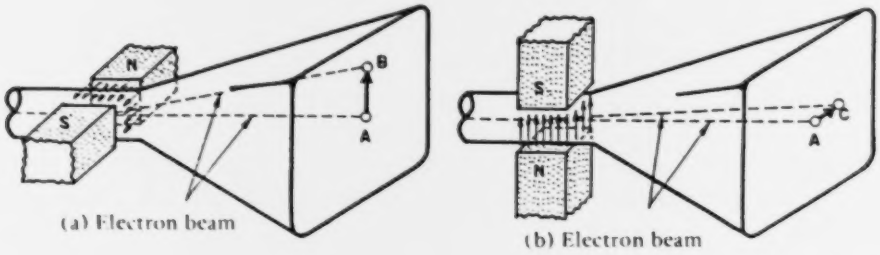


Figure 3-2
Principle of static deflection

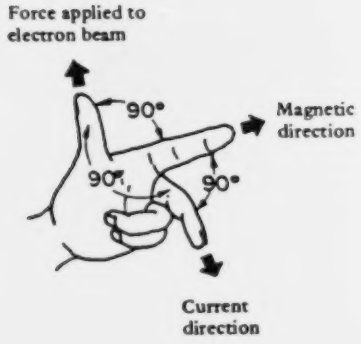


Figure 3-3
Flemming's left-hand rule

Magnitude of deflection (electromagnetic deflection)

The magnitude of deflection is proportional to the strength of the magnetic field and inversely proportional to the square root of the anode voltage.

To reproduce a linear picture, the strength of the magnetic field should vary linearly. The strength of the magnetic field (H) produced by the deflection coils is proportional to the product of the number of turns of the coils (N) and the current (I) flowing through them. Thus a greater value of NI means a stronger magnetic field and a larger deflection.

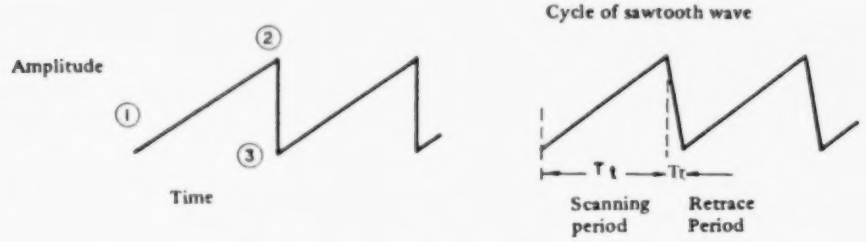
Sawtooth wave

Linear scanning of the CRT is achieved only if the electron beam is deflected linearly. This requires the current through the coils to be a linear sawtooth wave.

Figure 3-6(a) shows an ideal linear sawtooth wave. The wave can be divided into two sections: a) linear increase from its minimum to its maximum value and b) instant drop from its maximum to its minimum value.

It is impossible, however, to generate an ideal sawtooth wave, because zero decay time is just not possible. An actual sawtooth wave is shown in Figure 3-6(b).

A sawtooth wave can be divided into two sections: a) interval of the linear increase from its minimum to its maximum value (Tt, trace period) and b) interval of the sudden decrease from its maximum to its minimum value (Tr, retrace period).



(a) Ideal sawtooth wave (b) Sawtooth wave actually used

Figure 3-6
Sawtooth wave

Sawtooth generator circuit

Figure 3-7 shows the principle for generating a sawtooth wave. A sawtooth wave is generated by constantly charging and discharging a capacitor.

The circuit in Figure 3-7(a) will be used as an example to explain how a sawtooth wave is generated. Assume that capacitor C has no initial stored charges. When switch S is on, the supply voltage E_b charges C through resistor R. The voltage across C increases until it equals the supply voltage.

If S is switched off after C is fully charged, C immediately discharges. By constantly switching S on and off, a sawtooth wave is generated, as shown in Figure 3-7(b).

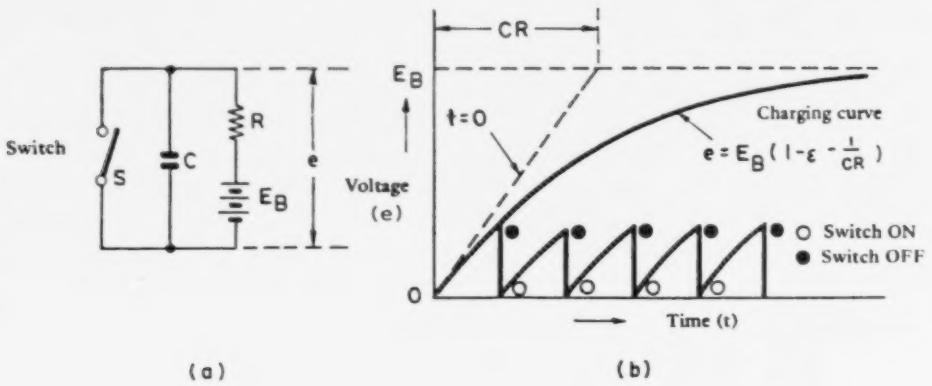


Figure 3-7
Basic sawtooth-wave generator circuit

Figure 3-9(a) shows a fundamental sawtooth-wave generator circuit. A transistor is used as a switch. The transistor is switched on during the interval when positive pulses are applied to the base, and is off between intervals of the pulses.

The transistor used in the sample circuit is an NPN type. A PNP transistor could have also been used, but the polarity of the keying pulses should be reversed. For this case, the polarity of the sawtooth wave is also reversed.

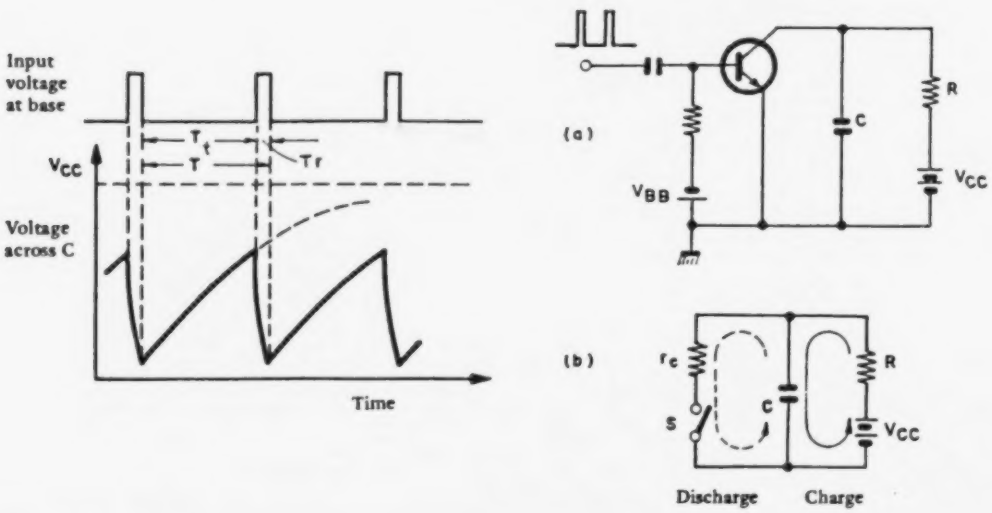
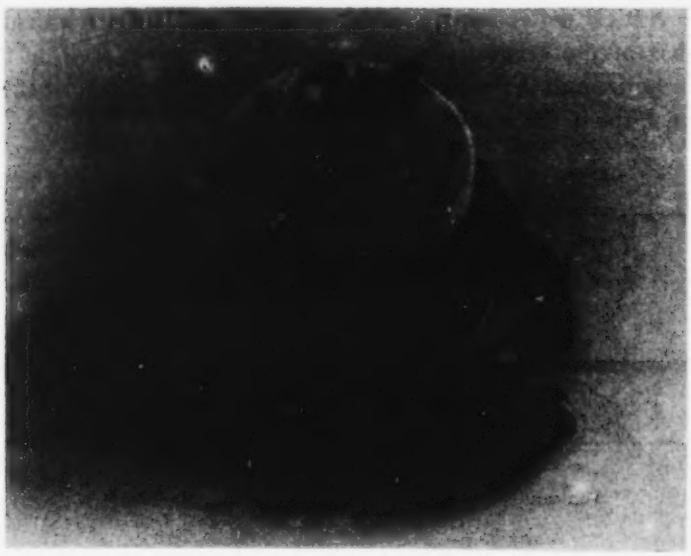


Figure 3-9
Sawtooth-wave voltage-generator circuit

Deflection coil

The deflection yoke mounted at the neck of the CRT consists of a pair of horizontal and vertical deflection coils. The current through each of these coils produces a magnetic field which deflects the beam from left to right and from top to bottom.

There are many kinds of deflection coils. Picture 3-1 shows one example. For delta gun CRTs the winding of the coil is designed to produce a constant electromagnetic field. For in-line gun CRTs the winding is designed to produce a distorted electromagnetic field to enable easy convergence adjustments for the three electron beams.



Picture 3-1
A deflection coil

Synchronisation circuits

Function of the sync signal

Image reproduction on the CRT screen must be synchronised precisely with the disassembly of the image in the camera at the broadcast station. Broadcast stations send vertical and horizontal sync signals with the luminance or video signal. The signals are processed by the sync circuits of the receiver for synchronisation.

The sync pulses synchronise the frequency of beam deflection in the CRT with the scanning frequency of the camera at the broadcast station. Thus the frequency of the sawtooth current through the horizontal and vertical deflection coils is equal to the frequency of the horizontal and vertical sync signals, respectively.

If the vertical deflection frequency (vertical oscillation frequency) is not equal to that of the vertical sync signal, the image reproduced on the screen rolls. If the horizontal deflection frequency is not equal to that of the horizontal sync signal, the image on the screen tears diagonally.

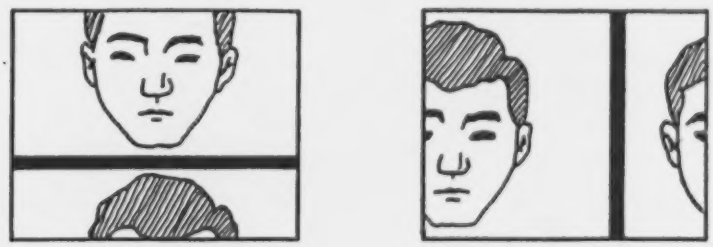


Figure 3-10
Phase relation of sync signals affecting reproduction of picture

Sync signals are multiplexed and transmitted with the luminance signal. The sync signals must be separated from the composite video signal before being supplied to the sync circuits. This prevents noise in the video information from affecting synchronisation of the receiver.

Sync separator circuits are used to separate the sync signals from the composite video signal. The sync signals are further separated into horizontal and vertical sync signals before they are finally supplied to their respective circuits. But if the composite video signal is supplied to the sync circuits, the luminance signal can trigger the oscillator circuits and affect synchronisation.

Amplitude separator circuit

The circuit used in separating the sync signal from the composite video signal is

an amplitude separator circuit. Figure 3-11 shows a basic amplitude separator circuit.

The composite video signal with negative polarity is coupled to the base of the sync separator transistor by C1. Time constant R1C1 is set to a large value. The circuit is biased so that only the sync signal triggers the transistor on. Thus, only the sync signals are amplified and taken at the output.

Let us see how the circuit works. During the retrace period, the sync pulse decreases the base voltage of the transistor and turns it on. Base current flows, charging the capacitor with the polarity indicated in the figure. Collector current also flows, producing an amplified sync signal at the output.

At the start of the trace period, C1 starts to discharge through R1. The polarity of the voltage across R1 due to the discharge is such that the base is positive with respect to the emitter. This turns off the transistor.

Because the transistor does not conduct, the luminance signal during the trace period is not amplified.

C1R1 is set to a large value to get a long discharge time. This keeps the transistor cut off during the trace period.

When the next sync pulse is supplied, the transistor turns on again, repeating the cycle. Therefore the output of the circuit consists only of the sync (horizontal and vertical) signals.

In an NPN transistor the polarity of the composite video signal supplied to the base should be positive. In this case negative sync signals are taken at the output.

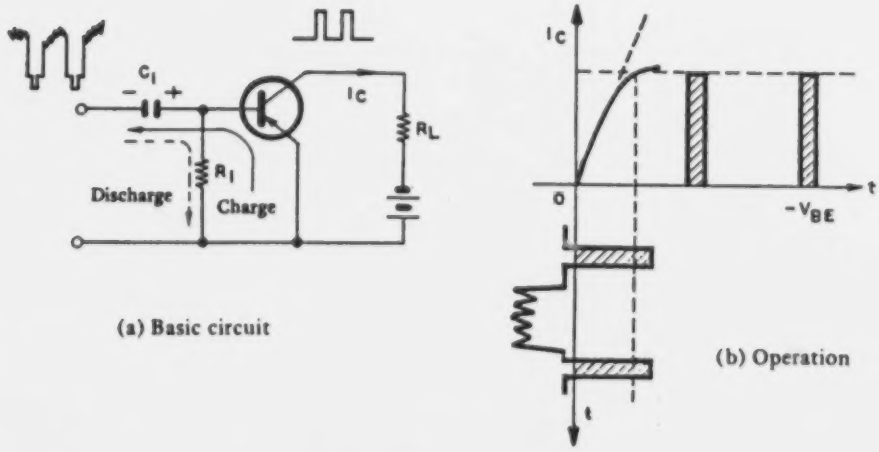


Figure 3-11
Sync separator circuit

Frequency separator circuit

The signal separated by the amplitude separator circuit consists of horizontal and vertical sync signals. These signals have to be further separated before they

are supplied to the horizontal AFC and vertical oscillator circuits, respectively. The vertical and horizontal signals are separated from each other by the frequency separator circuit. The vertical signal is taken from a low-pass filter, the horizontal signal from a high-pass filter.

Figures 3-13(a) and (b) show basic low- and high-pass filter circuits used in frequency separator circuits. The low-pass filter is called an integrator, since its output is integral to the input signal. The high-pass filter in (b) is called a differentiator, since its output derives from the input signal.

Integrator circuit. During the pulse periods the voltage across capacitor C increases rapidly from its initial value to its maximum value, which is equal to the peak of the pulse signal. The rate of increase in voltage across C is determined by time constant CR. During the interval between the pulse signals, C discharges.

Figure 3-13(b) shows the input and the corresponding output signal of the integrator circuit shown in (a).

Since the duration of the vertical pulses is much longer than that of the horizontal pulses, the charged voltage across C due to the horizontal pulses is negligible compared with voltage due to the vertical pulses.

Two to three stages of integrator circuits are used to filter the horizontal from the vertical sync pulses. This attenuates the horizontal pulses, since their presence in the vertical sync circuits affects vertical synchronisation.

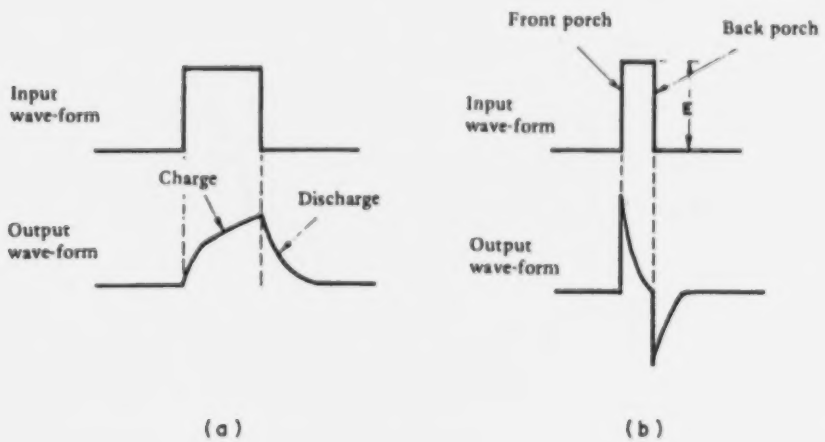
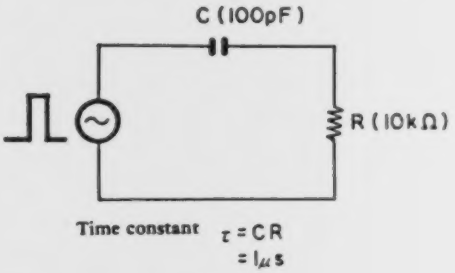


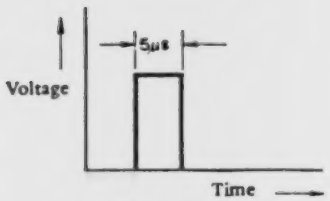
Figure 3-13
Frequency separator circuits

Differentiator circuit. This circuit, shown in Figure 3-15(a), is similar to a CR coupling circuit. But time constant CR of the circuit is smaller, usually around 0.8 to 1.0 usec.

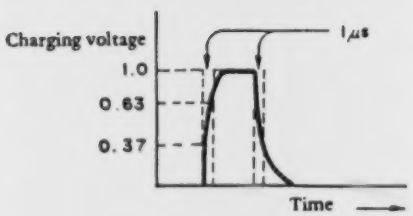
When the horizontal sync pulse in Figure (b) is applied, the capacitor is charged by the large current that flows during the front porch of the pulse.



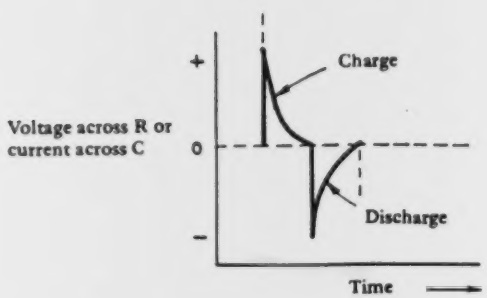
(a) Differentiator



(b) Input signal



(c) Voltage across C



(d) Current flow in the circuit

Figure 3-15
Differentiator circuit

Since time constant is 1 usec, the capacitor becomes fully charged in about 1.5 usec, long before the end of the 5 usec duration of the pulse.

The voltage across capacitor C with respect to time is shown in (c). The curve in (d) is the voltage across resistor R, which is the difference between the pulse and capacitor voltages.

Since the current through and the voltage across R have the same wave-shape, the curve above zero level in (d) is also the charging current.

After the duration of the pulse, C discharges through R. This discharge current is the curve below zero level in (d). It is negative, since the direction of the discharge current is opposite the direction of the charging current.

Figure 3-14(b) shows sync signals applied to the differentiator circuit and the output. In actual sync circuits the average of the horizontal sync signals is used to control the horizontal oscillator frequency.

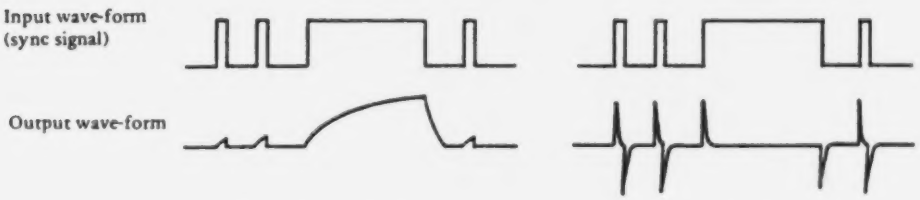


Figure 3-14
Input/output wave-form of the integrator and differentiator circuits

Noise-suppression circuit

Noise pulses picked up during the transmission of the TV signal greatly affect synchronisation of the receiver. Noise present in the composite video signal should be filtered before the signal is fed to the sync separator circuit. If noise is not filtered, it is taken by the sync separator circuits and supplied to the sync circuits. Noise triggers the oscillators and disrupts synchronisation.

A noise-suppression circuit is used to filter noise. Examples of such circuits are shown in Figures 3-16 and 17. The noise-suppression circuit in Figure 3-16 is formed by C2, R3 and D, which is a noise-clipping diode.

Positive composite video signals from the emitter of Q1 are supplied to the cathode of the diode.

The noise-clipping diode is forward-biased by R1 and R2 so the diode remains on during the sync pulses. However, noise in the composite video signal drives the cathode to a potential higher than the potential at (E), which reverse-biases the diode. Therefore, noise is clipped and not supplied to the sync separator transistor Q2.

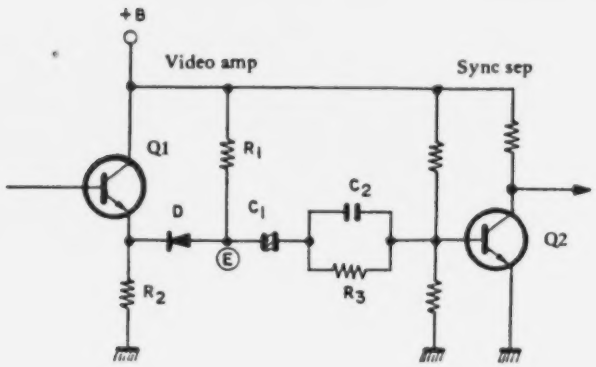


Figure 3-16
Noise-suppression circuit

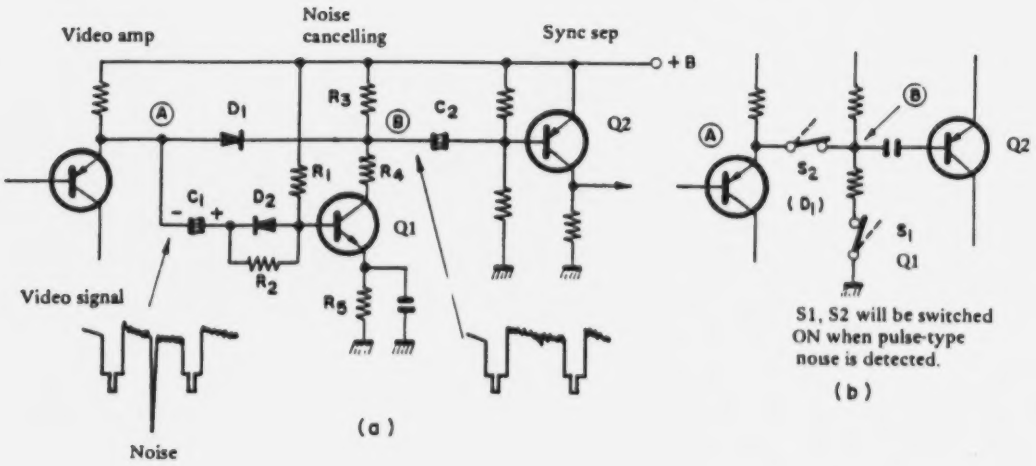


Figure 3-17
Noise-suppression circuit

Actual sync circuit used in TV receivers

Figure 3-18 shows an actual sync circuit. The sync separator circuit is usually connected to the emitter circuit of the video-amplifier transistor.

The low-output impedance of an emitter-follower circuit is needed to match the low-input impedance of the sync separator circuit during saturation.

In Figure 3-18 the noise separator circuit is connected before the sync separator and sync amplifier circuit. The sync amplifier performs phase-splitting, wave-form sharpening and noise reduction. Positive and negative sync signals needed for the balanced AFC circuit are supplied by the sync amplifier circuit.

Figure 3-19 shows a sync circuit using an IC. The IC functions as a) sync separator, b) noise suppressor, c) IF AGC, d) RF AGC, e) video amplifier and f) pulse amplifier.

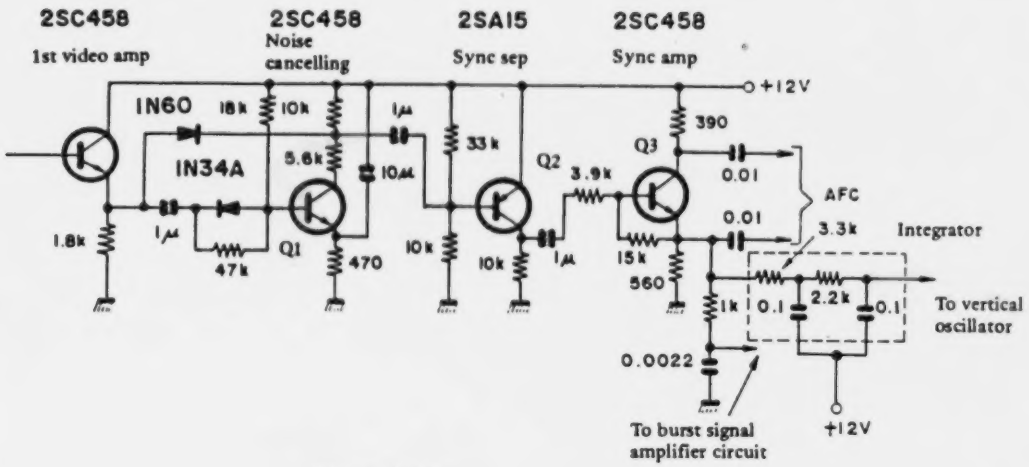


Figure 3-18
A sync separator circuit

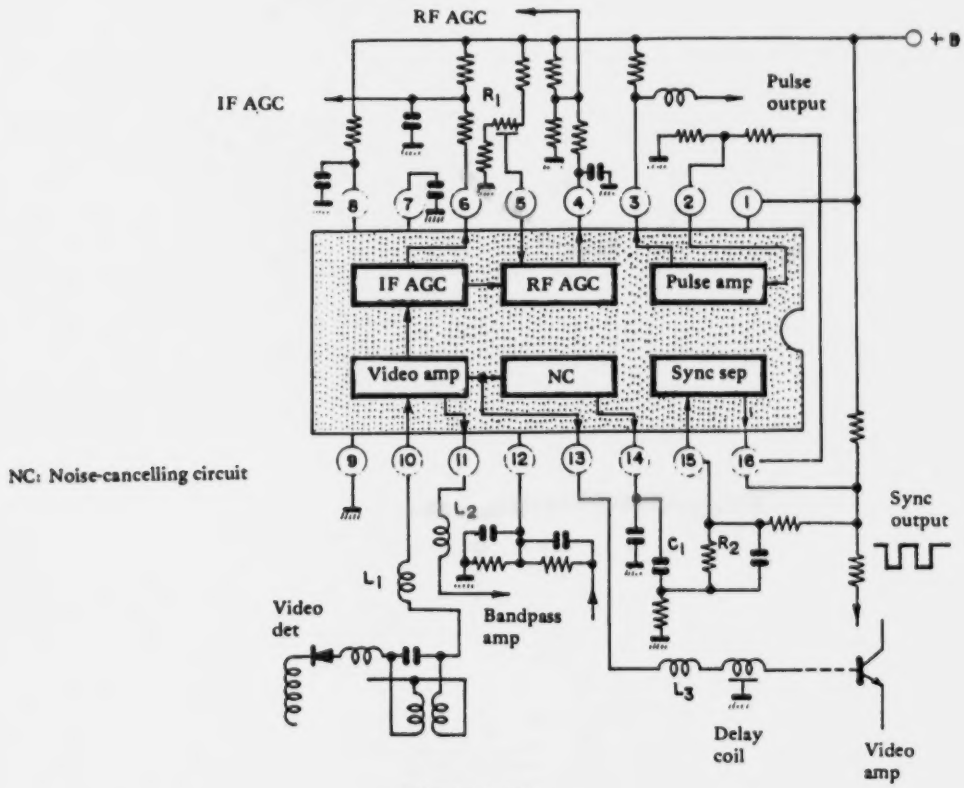


Figure 3-19
An IC sync separator circuit

The composite video signal taken from the video detector is fed to pin 10 and amplified by the video-amplifier circuit. The noise-suppressor circuit filters noise in the composite video signal. Pin 14 supplies a composite video signal free of noise. This signal is coupled to pin 15 by C1 and R2. The output is taken from pin 16 and fed to the horizontal AFC and integrator circuits.

Vertical deflection circuits (VDCs)

Block diagram of the VDC

Figure 3-20 shows a block diagram of the vertical deflection circuit (VDC), which consists of the vertical oscillator, vertical drive and vertical output circuits.

The vertical oscillator circuit generates a sawtooth voltage which is wave-shaped and amplified by the VDC. The vertical output circuit amplifies the voltage and supplies a sawtooth current to the vertical deflection coil. The frequency and phase of the vertical oscillator circuit are controlled by the vertical sync signal.

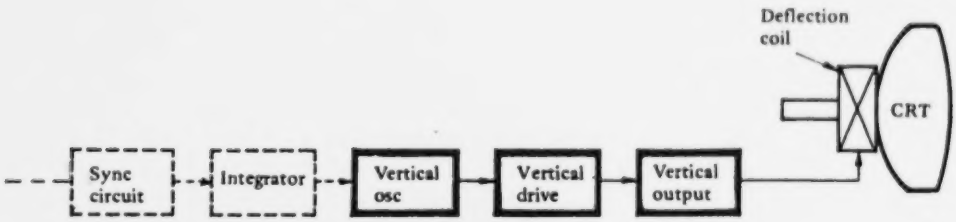


Figure 3-20
Functional block diagram of the vertical deflection circuit

Vertical oscillator circuit

A sawtooth voltage is usually generated by constantly charging and discharging a capacitor.

The vertical oscillator transistor is used as a switch which determines the cycle of the charging and discharging of the capacitor. It operates in the cut-off and saturation regions only. Either a blocking oscillator or a multivibrator is used in the vertical oscillator circuit.

Blocking oscillator circuit. Figure 3-21(a) shows a blocking oscillator used in a sawtooth voltage-generator circuit. The base and the collector of transistor Q are electromagnetically coupled by a blocking transformer. The sawtooth voltage is taken across R3.

When power is applied to the circuit, the voltage-divider network formed by R1 and R2 + VR supplies a positive voltage to the base of Q. At this instant a large initial charging current flows through C and R3. This current makes the emitter voltage more positive than the base, keeping Q cut off. But this current decreases as the capacitor is charged. As the current decreases, the emitter voltage also decreases.

Figure 3-21(b) shows a plot of the emitter voltage with respect to time. When the emitter voltage becomes less than the base voltage, the transistor conducts and the collector current increases.

The increase in collector current induces a voltage across L1, which in turn induces a voltage across L2. L2 is wound such that the polarity of this induced voltage tends to increase the base voltage.

Increasing the base voltage increases the collector current, which in turn

increases the induced voltage across L2 that tends to increase the base voltage. This is called positive feedback and continues until the transistor is saturated.

During saturation the capacitor discharges through Q and R3. The change in collector current during saturation is negligible, keeping the collector current practically constant.

When there is no change in the collector current, the induced voltage across L2 becomes zero and it decreases the base voltage to the DC base bias voltage. A decrease in the base voltage decreases the collector current and induces a voltage across L1, which in turn induces a voltage across L2. However, the polarity of the induced voltage this time tends to decrease the base voltage.

Decreasing the base voltage decreases the collector current, which in turn increases the induced voltage that tends to decrease the base voltage. This is negative feedback and continues until the transistor is driven to cut off.

The base voltage returns to its DC bias value. But the transistor remains cut off, because the capacitor starts to charge again, keeping the emitter more positive than the base. At this point the cycle is repeated.

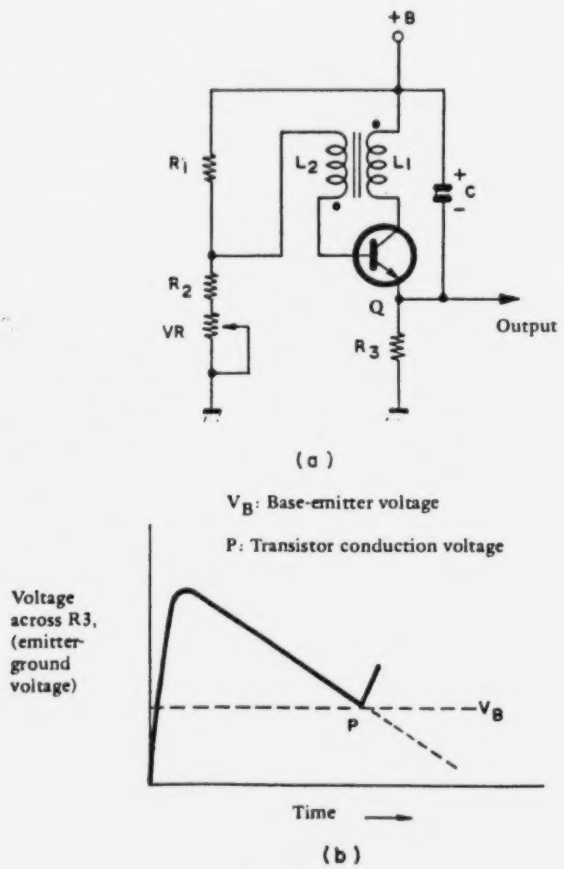


Figure 3-21
Blocking oscillator circuit used in a sawtooth generator circuit

This cycle generates a sawtooth voltage across R3. The frequency of this signal is controlled by time constant CR3. The linearity of the sawtooth voltage depends much on the value of CR3. Thus the frequency of the signal is varied by adjusting VR because the DC base bias voltage also affects the duration of the cycle.

Multivibrator circuit. Figure 3-22 shows another sawtooth voltage-generator circuit. This circuit uses a multivibrator for its oscillator. Instead of a transformer, as in the blocking oscillator, an amplifier circuit is used.

Q1 and Q2 are coupled by capacitors C1 and C2. When Q1 is on, its collector voltage turns off Q2. When Q2 is on, its collector voltage turns off Q1. The on-off period is determined by the time constant of the base circuit of each transistor.

The circuit enclosed by the broken line is the equivalent circuit of a sawtooth voltage generator. To generate the sawtooth voltage, use the pulse signal generated at the collector circuit of the multivibrator transistor Q2 to switch on and off a sawtooth voltage-generator transistor, or connect a capacitor at the collector circuit of Q1. In the latter, the sawtooth voltage is taken across C.

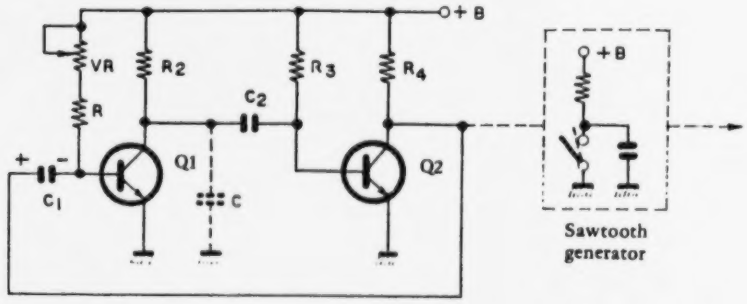


Figure 3-22
A multivibrator oscillator circuit

Other multivibrator circuits. Figure 3-23 shows another multivibrator used in a sawtooth voltage-generator circuit. This circuit uses a pair of PNP and NPN transistors. The collector of Q1 and the base of Q2 are coupled directly; the base of Q1 and the collector of Q2 are coupled capacitively.

When power is applied to the circuit, a positive voltage is supplied to the base of Q1 by the voltage divider network formed by R1 and VR. However, a more positive voltage supplied to the emitter drives Q1 into conduction.

The collector voltage of Q1 increases as it starts to conduct. The increasing collector voltage of Q1 turns on Q2. When Q2 conducts, an increase in its collector current decreases its collector voltage due to the increase in the voltage drop across R3.

Because C1 couples the collector of Q2 to the base of Q1, the base voltage of Q1 also decreases, making Q1 conduct more. As Q1 conducts more, the base voltage of Q2 increases. The two transistors are instantly saturated by this positive feedback. When both are saturated, C1 is charged with the polarity shown in Figure 3-23.

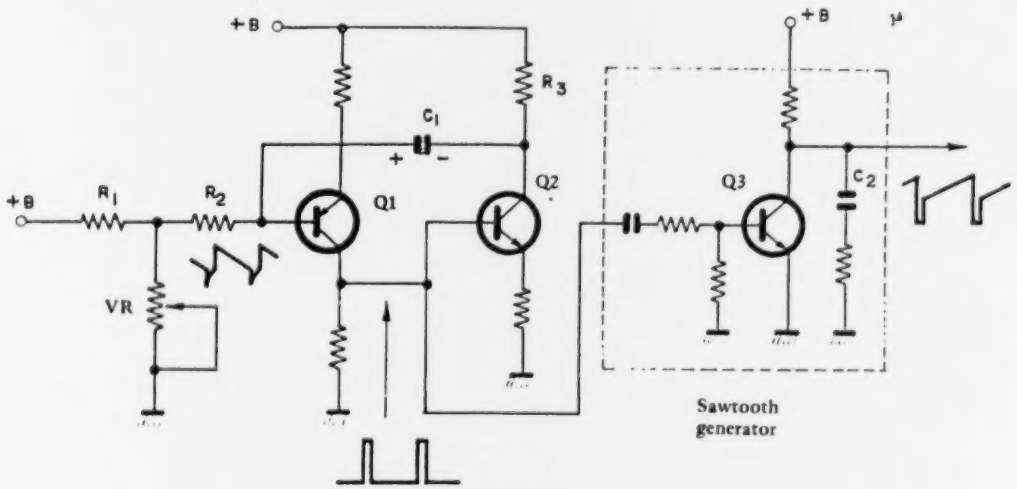


Figure 3-23
A sawtooth generator circuit with multivibrator

The charged voltage across C1 drives the base of Q1 positive. As C1 is charged, the base voltage increases until it exceeds the emitter voltage. When this happens Q1 is driven to cut off. As Q1 stops conducting, its collector current and voltage decrease. This turns off Q2.

When both transistors are off, C1 discharges through R1, R2, R3 and VR. As C1 discharges, the base voltage of Q1 decreases until its base-emitter junction is forward-biased and driven to conduction. Q1 then turns on Q2 and the cycle is repeated.

If the charging time of C1 is designed to be much less than its discharge time, a pulse signal is generated at the collector of Q1. This signal is used to switch Q3 on and off to generate a sawtooth voltage across C2 at the output.

Coupling the sync signal

There are two methods of controlling the frequency and phase of the vertical and horizontal oscillator circuits. One is by directly controlling the oscillator by injecting the sync signal directly to the circuit. This method is used in the vertical deflection circuit. The other method uses the average of the sync signal to control the horizontal oscillator. This is called sync AFC. This method is used in the horizontal deflection circuit.

Figure 3-24 shows a sync-signal coupling in a vertical blocking oscillator

circuit that uses an NPN transistor. The transistor is turned on by the positive sync signal supplied to the base of the transistor.

If a PNP transistor is used, the negative sync signal is used to turn it on. Without the sync signal applied to the base, the oscillation frequency of the circuit depends largely on the base voltage, as shown in Figure 3-25(a).

A lower base voltage yields a lower oscillation frequency, a higher base voltage a higher oscillation frequency.

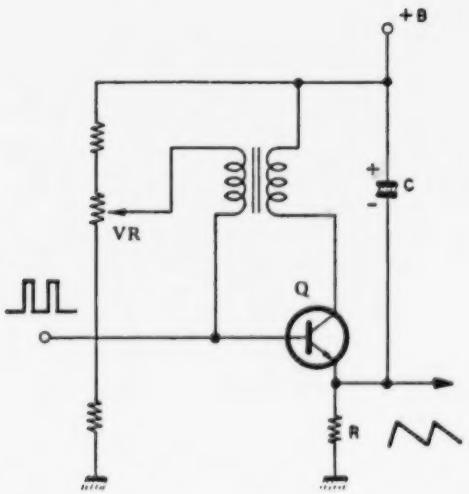


Figure 3-24
A sync-signal coupling circuit

When the oscillation frequency is set a bit lower than the frequency of the sync signal and the positive sync signal is applied to the base shortly before the emitter voltage or sawtooth voltage reaches its minimum, the pulse triggers the transistor on. This sets the frequency and phase of the sawtooth voltage equal to the frequency and phase of the sync signal.

In Figure 3-25(b) the solid sawtooth wave is the output if the sync signal is applied. The dashed wave is the output if the sync signal is not supplied to the base.

Vertical drive circuit

The strength of the sawtooth voltage produced in the vertical oscillator circuit is not enough to drive the vertical output circuit.

The vertical drive circuit is used to increase the sawtooth voltage enough to drive the vertical output transistors. The vertical drive circuit also improves the linearity of the voltage.

The output of the vertical drive circuit should be enough to provide an adequate negative feedback to stabilise the entire vertical deflection circuit.

Sufficient output improves the linearity of the sawtooth voltage as well as the linearity of the raster. A common-emitter or an emitter-follower is used in the vertical drive circuit.

Figure 3-26 shows a common-emitter vertical drive circuit. VR1 functions as the vertical-size control by varying the amplitude of the sawtooth voltage.

If the sawtooth current flowing through the deflection coil is distorted, the upper or lower part of the raster will be stretched or compressed. The vertical drive circuit solves this problem by improving the linearity of the sawtooth current.

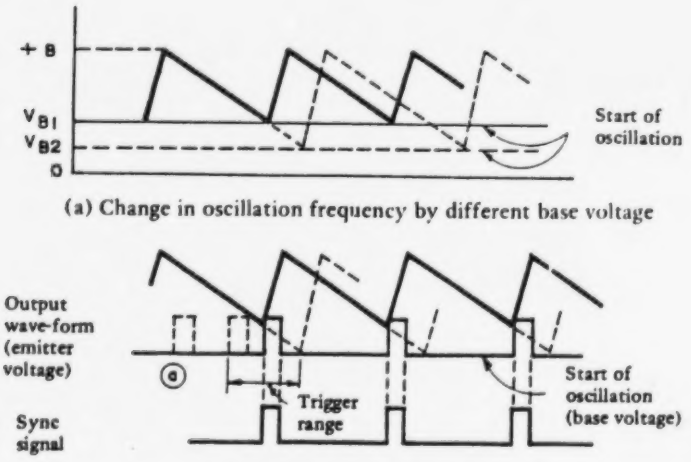


Figure 3-25
Synchronisation of oscillator frequency

The distortion of the current can be caused by 1) distorted oscillator wave-form, 2) transistor with poor linearity and 3) poor output transformer characteristic.

Many compensation circuits can remove distortion, but poor linearity is mainly corrected by negative feedback. Negative feedback is commonly obtained by connecting an emitter resistor to the vertical output circuit. Another method is to allow the deflection coil current to flow through the emitter resistor of the vertical drive transistor.

Special compensation and negative feedback circuits with an integrator are used to improve the oscillator wave-form.

Vertical output circuit

This circuit supplies the sawtooth currents to the deflection coils. The circuits shown in Figures 3-27 and 3-28 are commonly used. Figure 3-27 shows a common-emitter amplifier circuit. The output transformer is used to couple the output circuit to the deflection coil. This circuit is a class-A amplifier with an output power of just a few watts. However, this should be a high-powered transistor because a high-pulse voltage, whose strength is several times more than the

power-supply voltage, is generated during the retrace period and coupled to the collector. This high-pulse voltage is generated because of the inductance of the deflection coil.

A pulse-voltage-limiting circuit is included to limit the magnitude of the voltage generated and to protect the output transistor.

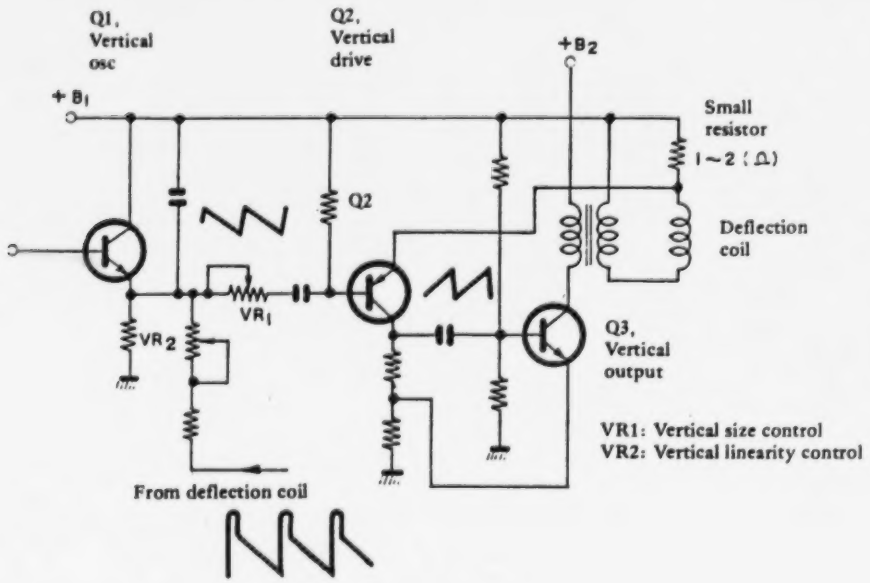


Figure 3-26
Common-emitter vertical drive circuit

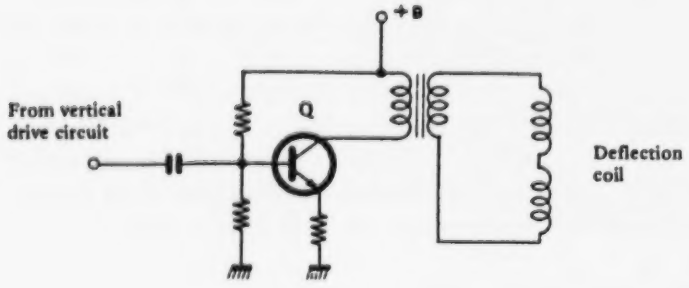


Figure 3-27
Common-emitter vertical output circuit

Figure 3-28 shows a single-end push-pull (SEPP) vertical output amplifier circuit. The output transformer is no longer necessary in this circuit.

This circuit is commonly used because the linearity of the sawtooth current flowing through the deflection coil is not easily distorted.

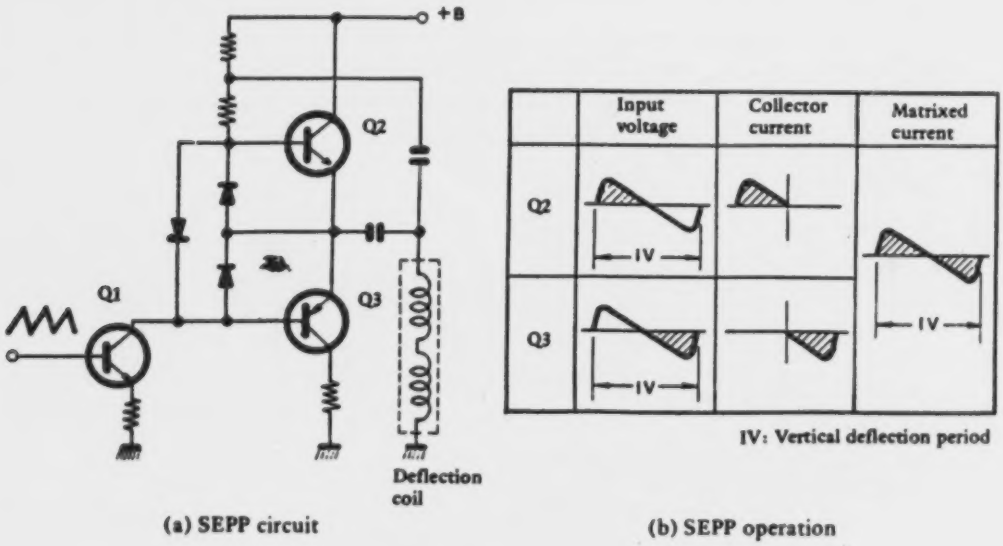


Figure 3-28
SEPP vertical output circuit and its function

Q1 is the vertical drive transistor, Q2 and Q3 are the vertical output transistors. The output transistors (NPN and PNP) complement the circuit.

The sawtooth voltage from Q1 is applied to Q2 and Q3. Q2 is on and conducts during the half-cycle of the scanning period, as shown in Figure 3-28(b). After the first half-cycle of the scanning period, Q3 is on and conducts. Both transistors are turned on alternately.

The collector currents of both transistors are combined to form the current supplied to the deflection coil to deflect the electron beam vertically. Because the transistors form a push-pull circuit, their characteristics must be the same.

The high-pulse voltage generated during the retrace period saturates both transistors. The internal resistance of the transistors during saturation is very low. In effect, the transistors function as low resistance parallel to the deflection coil. This lessens the magnitude of the generated pulse voltage, eliminating the need of a protection circuit for the output transistor.

Examples of actual vertical deflection circuits

Figures 3-29 and 3-30 show actual vertical deflection circuits. The circuit shown in Figure 3-29 uses a blocking oscillator.

A transformer-coupled class-A amplifier circuit is used as an output circuit. The linearity of the sawtooth voltage is improved by the negative feedback from the output and integrator circuit.

The thermistor (TH), connected to the base circuit of the output transistor Q3, is used for bias stabilisation.

The diode in the collector circuit absorbs the pulses which are generated during the retrace period.

The vertical centre position of the raster is adjusted by the variable resistor marked V-CENT and which is connected to the secondary of the vertical output transformer (VOT). It forms a bridge circuit with the secondary.

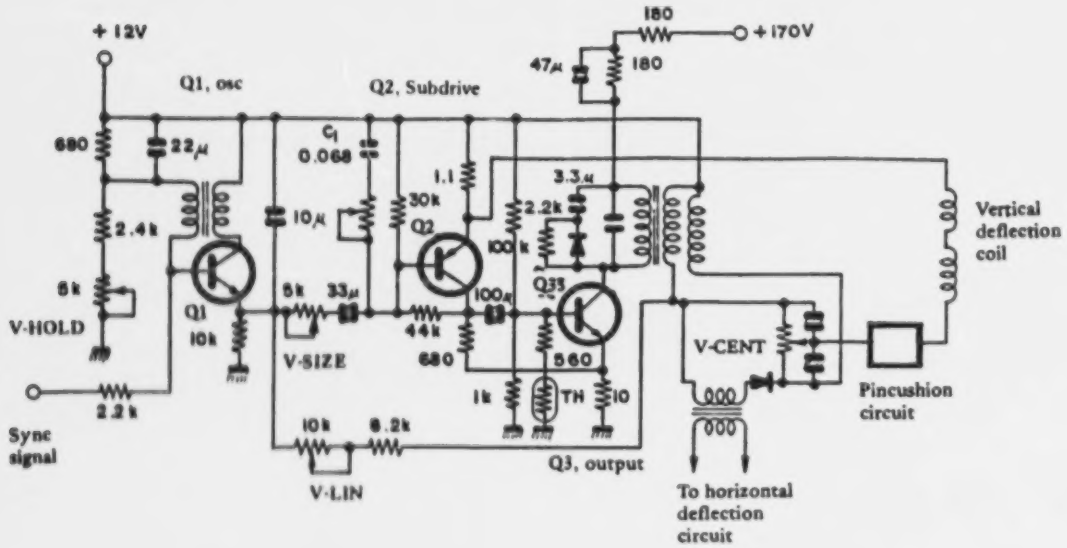


Figure 3-29
A vertical deflection circuit

By adjusting V-CENT, one varies the DC current flow in the deflection coil, changing the vertical position of the raster.

The vertical deflection circuit in Figure 3-30 uses a multivibrator circuit as the vertical oscillator circuit.

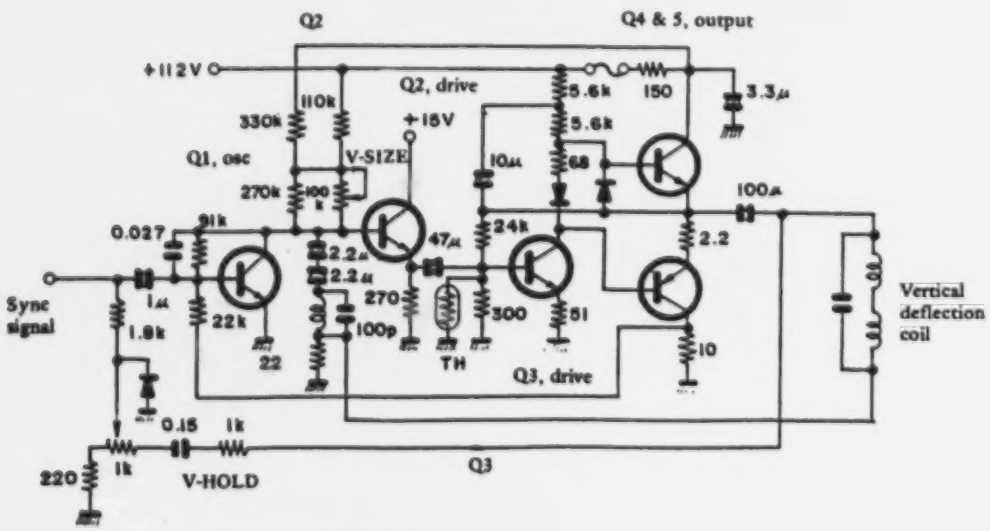


Figure 3-30
A vertical deflection circuit

A SEPP complementary circuit is used as the output circuit. This vertical deflection circuit has a dual vertical-drive stage.

Q1 functions as a switch in generating a sawtooth voltage.

Compensating circuits to improve linearity are omitted due to good response and matching of the SEPP and the deflection coil.

Horizontal deflection circuits (HDCs)

Block diagram of a horizontal deflection circuit

The sawtooth current supplied to the horizontal deflection coil has a frequency of 15,750 Hz.

Figure 3-31 shows a functional block diagram of the horizontal deflection circuit. It consists of the horizontal oscillator, horizontal drive and horizontal output circuits, the AFC, high-voltage generator and power-supply circuits.

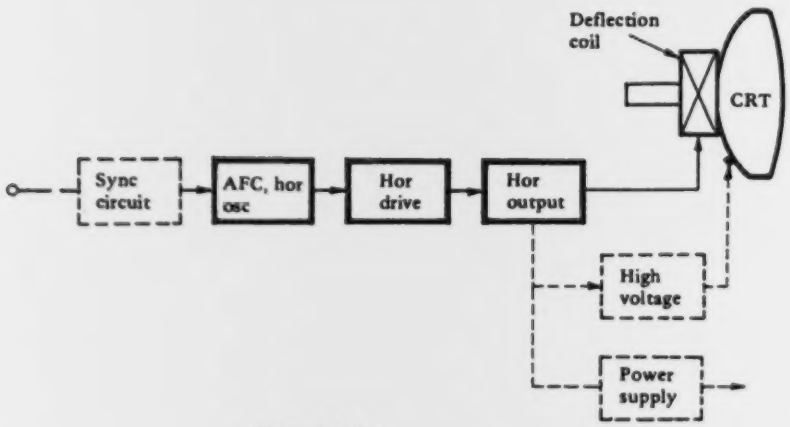


Figure 3-31
Functional block diagram of a horizontal deflection circuit

Synchronisation AFC circuit and its function

As mentioned in the section on "Frequency Separator Circuit," the vertical sync signal controls the vertical oscillator frequency. This signal is processed by two to three stages of low-pass filter (integrator) circuits that filter horizontal sync signal and noise. The vertical sync signal is then supplied to the vertical oscillator transistor.

On the other hand, the horizontal sync signal is processed by a high-pass filter circuit.

Noise between horizontal sync pulses in the TV signal (Figure 3-32) disturbs horizontal synchronisation and causes an unsteady image.

Figure 3-33 shows an example of noise interference in direct horizontal synchronisation.

In Figure 3-32 noise lower than the trigger level of the horizontal oscillator will not create interference on the screen. But noise greater than the trigger level of the horizontal oscillator will interfere with horizontal synchronisation and distort the image on the screen.

Figure 3-34 shows an image with partial loss in horizontal sync.

Noise creates distortion if the horizontal sync circuits are designed to use each of the pulses in the horizontal sync signal as a trigger signal to synchronise the horizontal oscillation with the horizontal scanning frequency.

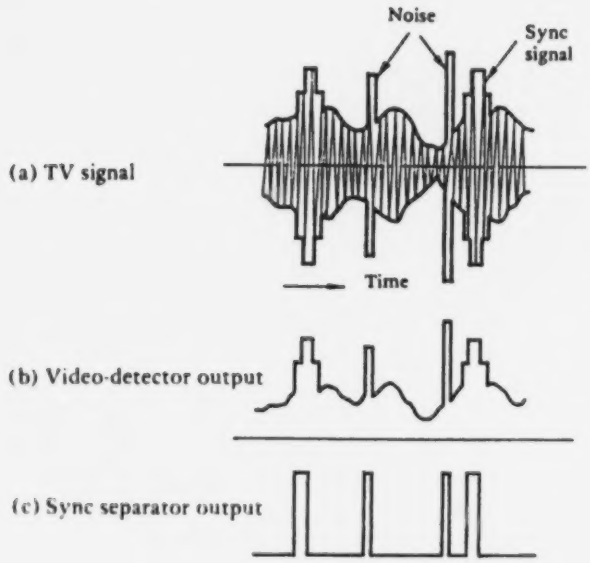


Figure 3-32
Noise between horizontal sync pulses in the TV signal

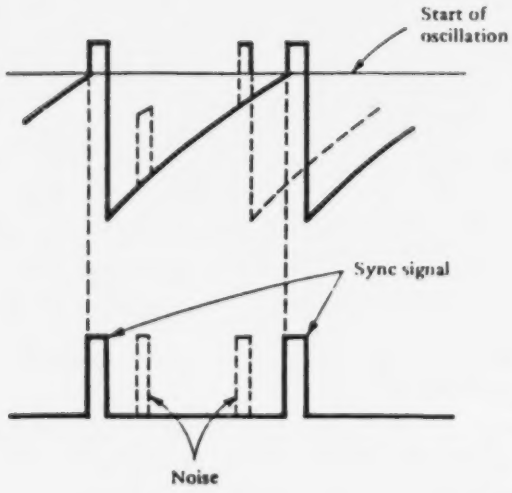


Figure 3-33
An example of noise interference in direct horizontal synchronisation

If the sync circuits are designed to respond only to the average of the horizontal sync signal per frame of video information, interference of noise with horizontal synchronisation is minimised. This is because the average of the sync signal is insignificantly affected by the presence of noise. Thus even continuous noise created internally by the receiver does not interfere with horizontal synchronisation of the receiver.

The horizontal sync circuit designed to respond to the average of the horizontal sync signal is called the sync AFC circuit. Its functional block diagram is shown in Figure 3-35.

This circuit consists of a phase detector, integrator, horizontal oscillator and comparator signal generator circuits.

The phase-detector circuit compares the phase of the retrace period of the sawtooth signal (sample signal) with the phase of the horizontal sync signal. When a phase-difference is detected, the detector produces a signal proportional to the difference. This signal is generally a pulse voltage filtered by the integrator circuit before being supplied to the horizontal oscillator circuit as the AFC-control voltage. The control voltage in turn adjusts the phase of the oscillator.

(a) Correct reproduction (b) Disturbed reproduction

Figure 3-34
Partial loss of horizontal synchronisation by external noise

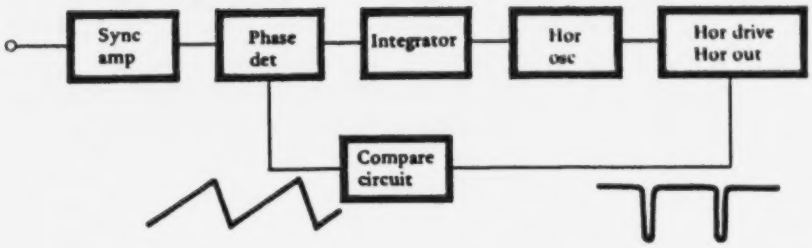


Figure 3-35
Functional block diagram of a sync AFC circuit

The polarity of the control voltage depends on the phasing of the signals. A positive control voltage is produced if the phase of the sample signal is faster (higher frequency) than the horizontal sync signal.

A special oscillator circuit is designed for the horizontal oscillator in which its phase and frequency can be controlled by the AFC-control voltage.

The sawtooth-wave AFC circuit is commonly used for the horizontal AFC circuit in TV receivers.

Balanced sawtooth-wave AFC circuit. Figure 3-36 shows a balanced sawtooth-wave AFC circuit. This circuit uses a geometric phase-detector circuit. It requires positive and negative sync signals as reference signals. These signals are taken from the sync amplifier circuit.

The control voltage which varies the horizontal oscillator frequency is produced by the AFC circuit and is generally supplied to the blocking oscillator circuit.

In Figure 3-36 positive and negative sync signals are taken from the collector and emitter circuits, respectively, of the sync amplifier transistor.

The horizontal flyback pulses are transformed into a sawtooth signal by the integrator circuit (C3, R3) and supplied to the junction of phase-detector diodes D1 and D2 as a sample signal.

The horizontal sync signals are supplied to D1 and D2 as reference signals.

The output voltage taken between the junction of R1 and R2 is the control voltage. The control voltage is supplied to the base of the horizontal oscillator transistor through an integrator circuit.

The details in operating a balanced sawtooth-wave AFC circuit follow.

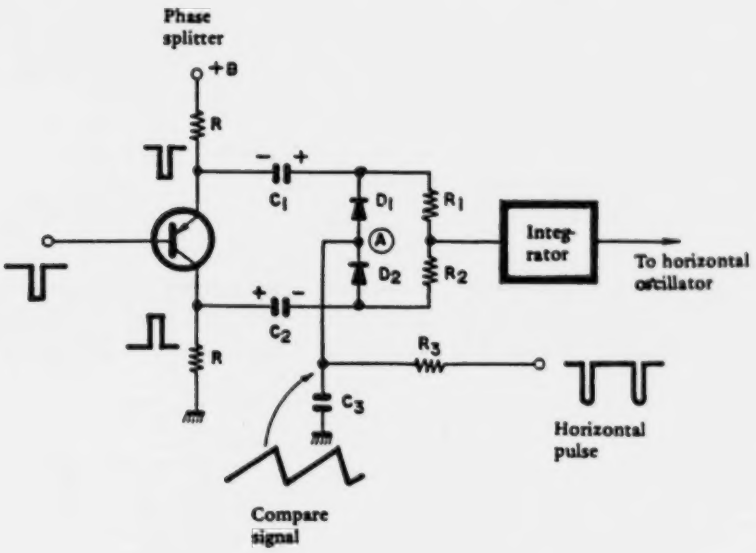


Figure 3-36
Balanced sawtooth AFC circuit

When the sample signal is not supplied. In Figure 3-37 the magnitudes of the sync signals applied to the phase-detector diodes D1 and D2 are equal. These signals charge C1 and C2 with equal magnitudes but opposite polarities. During intervals between sync pulses, C1 and C2 discharge through R1 and R2. But since C1 and C2 are charged equally, the voltage at point (B) due to the discharge of the capacitors is zero. Thus the AFC-control voltage is zero.

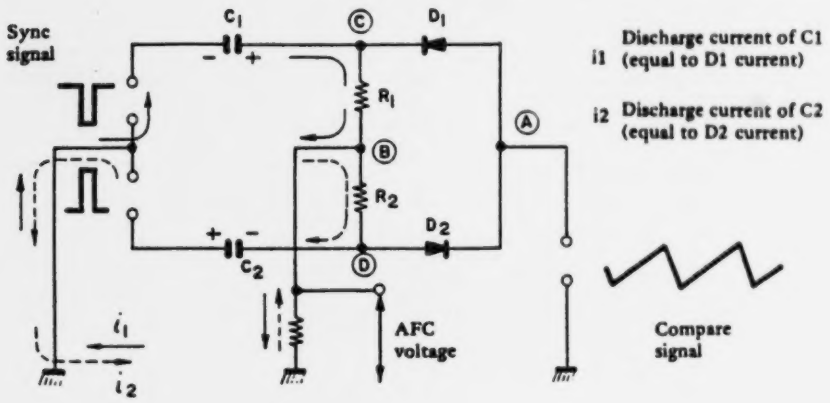


Figure 3-37
Signal process in a phase-detector circuit

When the sample signal is applied. When the sample signal is applied, the magnitudes of the currents through D1 and D2 depend on the possible phase relations between the horizontal sync signal and the sample signal, as shown in Figure 3-38.

The phase of the sample signal lags behind the sync signal when the horizontal oscillator frequency decreases, as in (a). Here the sync signals overlap with the sample signal at the beginning of the retrace period, and the signal detected by D1 becomes greater than the signal detected by D2. Thus C1 is charged with a magnitude greater than C2. When they discharge, the AFC-control voltage produced at point (B) in Figure 3-37 is positive.

On the other hand, when the horizontal oscillator frequency increases, as in Figure 3-38(c), the sync signal overlaps with the sample signal later during the retrace period. Here the voltage produced at point (B) when the capacitors discharge is negative.

The case shown in (c) is the proper phase relation. The signals detected by D1 and D2 are equal, thus producing no control voltage at point (B).

Figure 3-39 shows the relationship of the output voltage of the AFC circuit to the phase difference between the sample and sync signals.

The output voltage is integrated (filtered) and supplied to the horizontal oscillator circuit to control the horizontal oscillator frequency.

Unbalanced sawtooth-wave AFC circuit. Figure 3-40 shows an unbalanced sawtooth-wave AFC circuit. Unlike the balanced AFC circuit, it requires only a negative sync signal as reference signal.

Consider first the operation of the circuit when the sync signal is not supplied. When the sample signal is supplied, the diodes conduct alternately. D1 conducts during the positive cycle and D2 during the negative cycle. The direction of the current flow in the circuit during the positive cycle is indicated by the solid curve; the dashed curve indicates the direction of the current flow during the negative cycle.

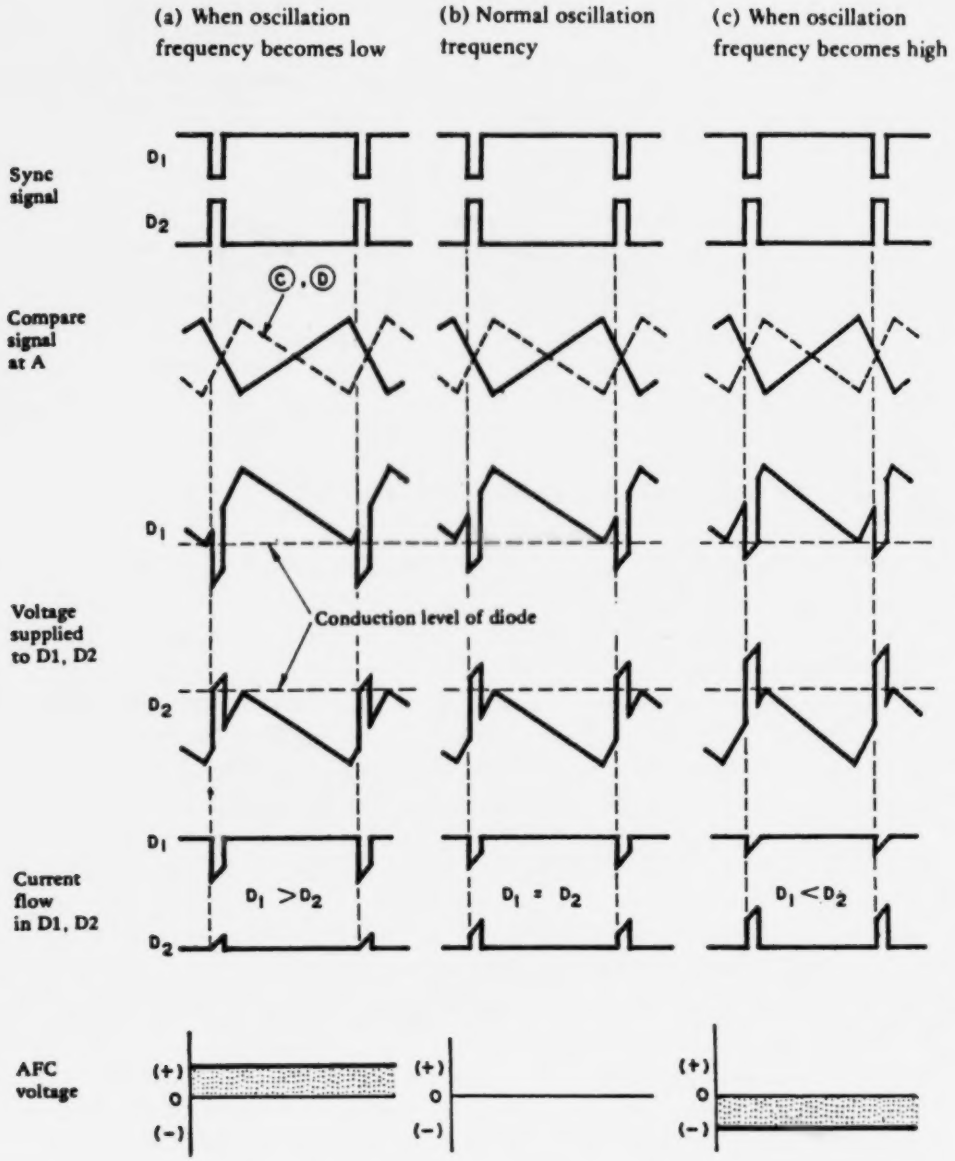


Figure 3-38
Phase relations between horizontal sync signal and sample signal

The currents flowing through D1 and D2 during each half-cycle are equal. C2 is charged alternately by the currents flowing through the diodes. But since the direction of the currents though each diode is opposite, the charged voltage across C2 in a complete cycle is zero.

Consider now the circuit when the sync signal is applied. The sync signal overlaps with the sample signal. Depending on the phase of the sample signal with respect to the sync signal, the current through D1 may be equal to, greater or less than the current through D2.

When the oscillator frequency changes, the corresponding control voltage is produced across C2 and integrated before it is supplied to the horizontal oscillator transistor as an AFC-control voltage.

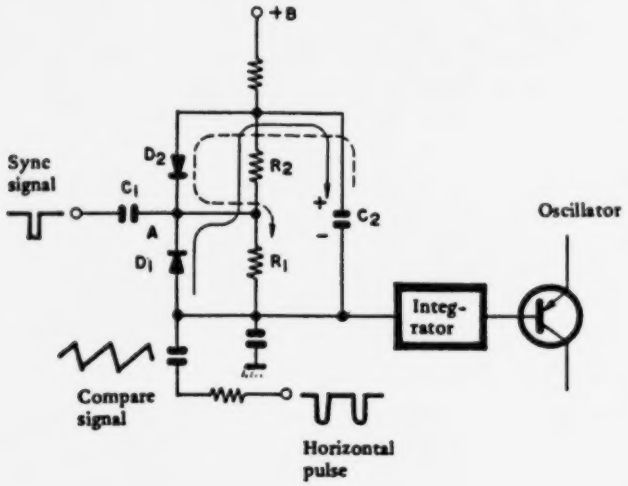


Figure 3-40
Unbalanced sawtooth AFC circuit

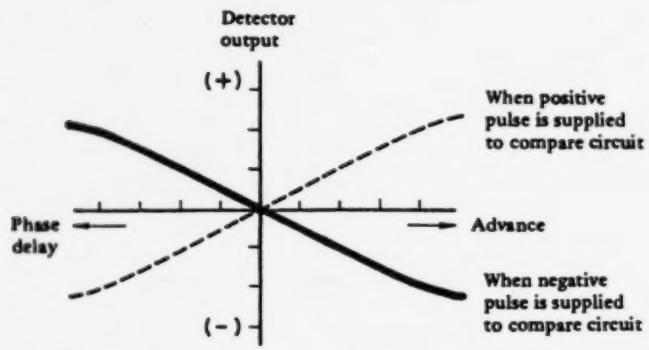
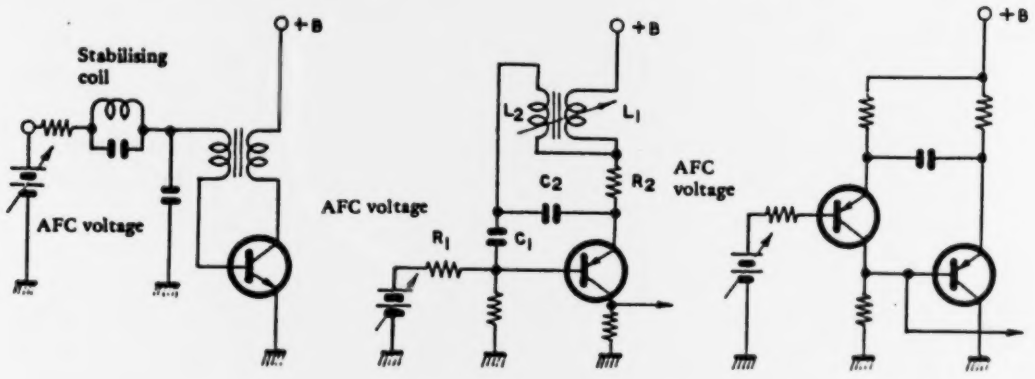


Figure 3-39
Relationship of AFC output voltage to the phase difference between the sample and sync signals

Horizontal oscillator circuit

Oscillator circuit. Several types of horizontal oscillator circuits are shown in Figure 3-41. The circuits in (a) and (b) use a blocking oscillator, the circuit in (c) an emitter-coupled multivibrator.



(a) Blocking oscillator (1) (b) Blocking oscillator (2) (c) Emitter-coupled multivibrator

Figure 3-41
Horizontal oscillator circuit

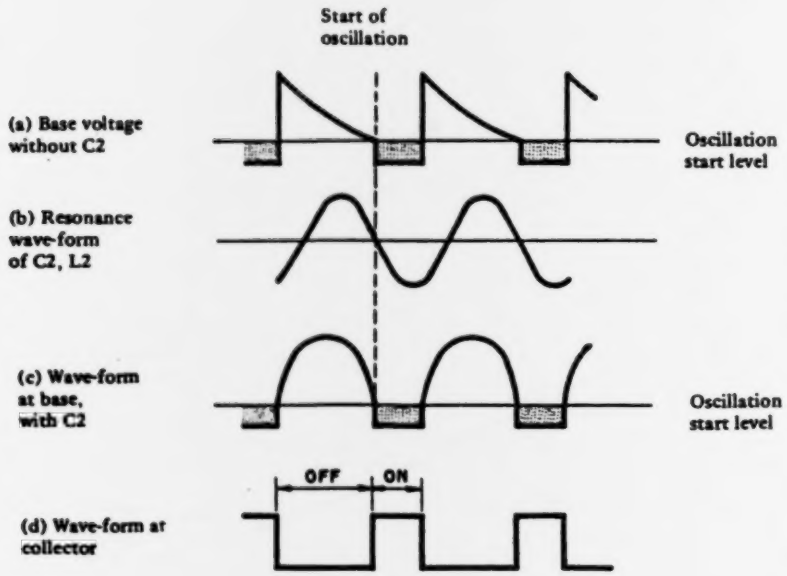


Figure 3-42
Functional wave-form in the blocking oscillator circuit

The horizontal oscillator circuit shown in (b) is commonly used because of its simplicity and inherent stability. This circuit combines a blocking oscillator with a Hartley oscillator circuit. L2 and C2 form a resonant circuit with a frequency of 15,750 Hz.

If C2 is removed from the circuit, the base voltage will be a sawtooth wave like the one shown in Figure 3-42(a). If the signal in Figure 3-42(b) which is

generated by the resonant circuit formed by L2 and C2 is mixed, the wave-form in (c) is generated at the base. In (c) the slope of the oscillator wave-form at the start of each cycle is very steep.

The signal is protected from noise interference and the oscillation remains stable even during variations in power supply and temperature.

Control of oscillator frequency. The oscillator frequency of the blocking and the multivibrator oscillator circuits depends on the time constant of the circuit and on the supply and base voltages.

If the time constant of the circuit and the supply voltage are fixed (or maintained constant), the oscillator frequency can be varied by the base voltage or the AFC-control voltage.

Figure 3-43 shows how the AFC voltage controls the oscillator frequency. When the AFC voltage is high, C discharges rapidly, resulting in less time between each oscillation. Thus the oscillation frequency is high.

When the AFC voltage is low, C discharges gradually, resulting in longer time between each oscillation. Thus the oscillation frequency is low.

Figure 3-44 shows the relationship of the AFC voltage to the oscillator frequency in a circuit where the time constant is fixed.

The explanation for a circuit using an NPN transistor is similar, but the effects of the AFC voltage on the oscillation are opposite.

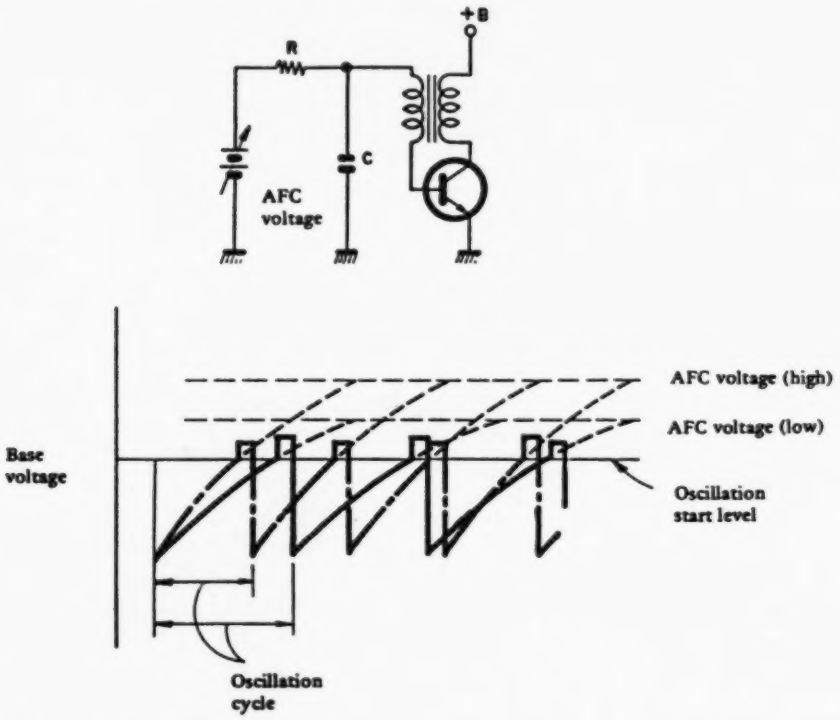


Figure 3-43
Oscillator frequency controlled by an AFC voltage

Horizontal drive and output circuit

Horizontal drive circuit. As explained in the following chapter, the horizontal output transistor functions as a mere switch to the horizontal deflection coil. Therefore, sufficient base current has to be supplied to the horizontal output transistor so that it can shift from saturation (ON state) to cut-off (OFF state) and vice versa rapidly.

For a supply of sufficient base current, an amplifier is placed between the oscillator and the horizontal output circuit to amplify and improve the output signal of the oscillator circuit. This amplifier circuit is called the horizontal drive circuit. Figure 3-45 shows a horizontal drive circuit. A transformer-coupled common-emitter amplifier circuit is commonly used.

The horizontal drive transistor operates like the horizontal output transistor. Both operate like a switch.

The horizontal output and drive circuits are designed to alternate each transistor as the load of the drive transformer. Thus when the output transistor is ON, the drive transistor is OFF; when the output transistor is OFF, the drive transistor is ON.

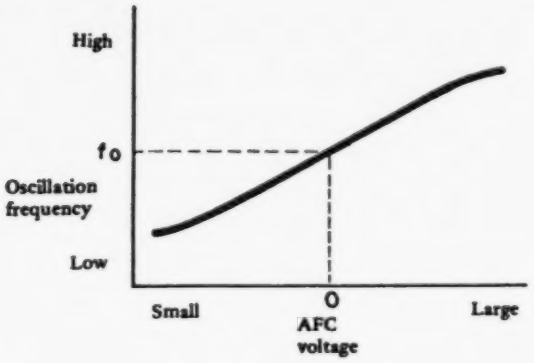


Figure 3-44
Relationship between AFC voltage and oscillator frequency

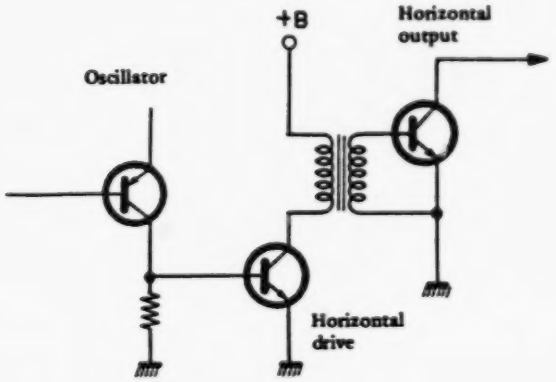


Figure 3-45
Horizontal drive circuit

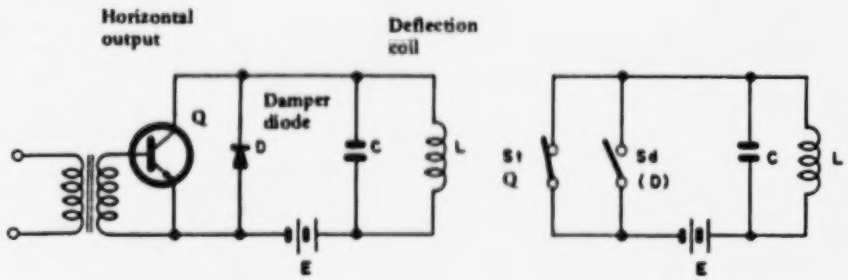
Horizontal output circuit. Figure 3-46(a) shows a horizontal output ciruit. The transistor in the circuit is used as a switch.

Combining a transistor with a damper diode produces a sawtooth current for the horizontal deflection coil.

The horizontal output transistor is triggered on by the pulse voltage applied to its base, and the damper diode conducts whenever the polarity of the stored charge in C supplies a forward-biasing voltage.

Because both the transistor and the damper diode function as a switch, the operation of the circuit can be explained using the equivalent circuit shown in Figure 3-46(b).

The horizontal deflection coil can be considered a series connection of its inductance L and its internal resistance r. But the internal resistance r is so small that the time constant L/r becomes large. Thus a rapidly changing voltage across the coil produces a sawtooth current through it.



(a) Basic circuit (b) Equivalent circuit

Figure 3-46
Horizontal output circuit

Details in the operation of the horizontal output circuit. Figure 3-47 shows a wave-form analysis of the horizontal output circuit.

[t1 - t2 period]

When the trigger voltage is applied to the base of the horizontal output transistor, sufficient base current flows and saturates the transistor. The transistor acts as a closed switch St, as shown in the equivalent circuit in Figure 3-46(b).

During saturation, the current starts to flow from the power source E to the deflection coil. But the current gradually and linearly increases due to the large time constant of the deflection coil.

[t2 - t3 period]

The horizontal output transistor is driven to cut off by the large negative voltage supplied to the base during this period. The transistor acts like an open switch.

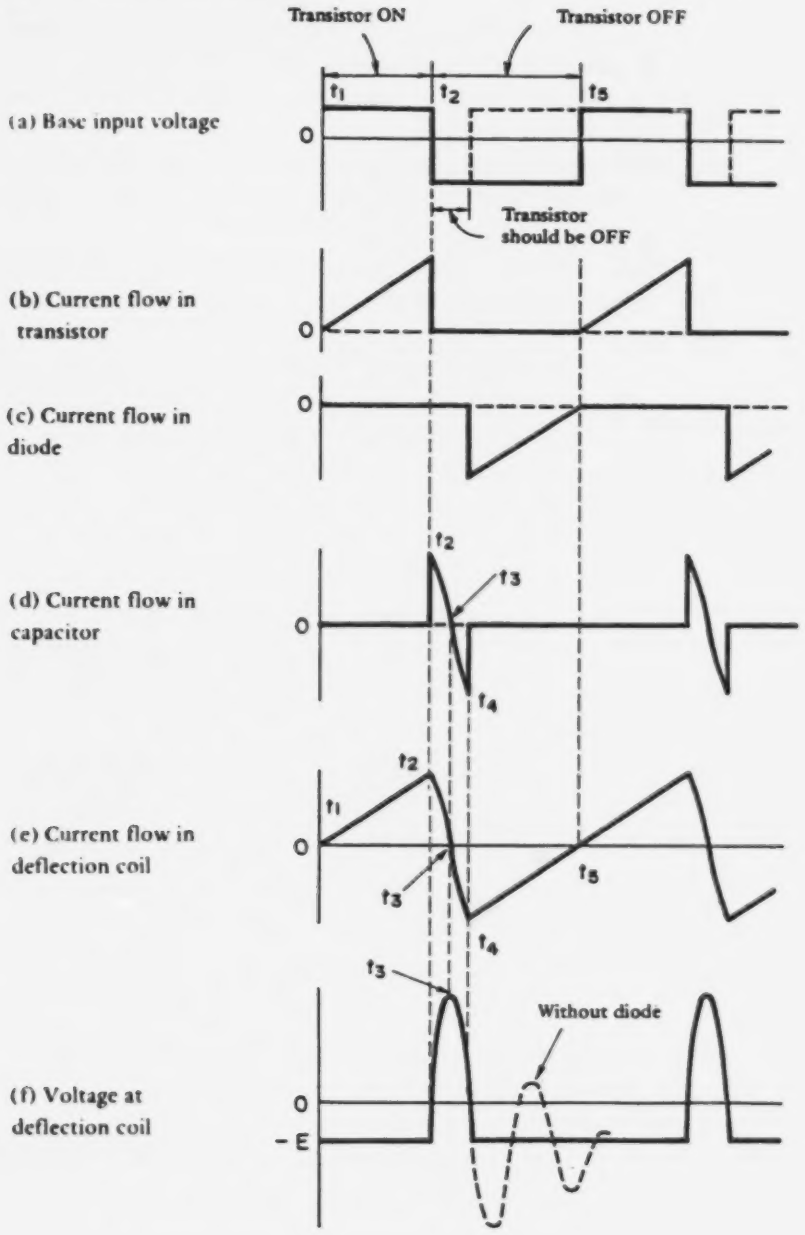


Figure 3-47
Wave-form analysis of the horizontal output circuit

The deflection coil and the capacitor (C) form a resonant circuit. When the current flow through the coil is suddenly stopped by cutting off the transistor, a voltage is induced across the coil.

The polarity of the induced voltage is shown in Figure 3-48(d). The induced voltage produces a current flow through C, whose wave-form is shown in Figure 3-47(d).

At t3 the current through C becomes zero. At this time C is fully charged and the voltage across it becomes maximum. This maximum voltage is called the "flyback pulse voltage."

[t3 - t4 period]

During this period C discharges through the deflection coil. The current through the coil and C reverses in direction. The current through the coil increases as the stored charge in C decreases. The current becomes maximum at t4 when the voltage across C decreases to zero. Right after C completely discharges, it is charged again.

The transfer of energy is only between L and C, since the damper diode is reverse-biased. Thus the circuit will oscillate at a resonant frequency determined by the values of L and C.

[t4 - t5 period]

At t4 the voltage across C (also across L) is zero, and the current flowing through the coil is maximum. This current charges C in a polarity opposing the supply voltage.

When the voltage across C exceeds the supply voltage, the damper diode becomes forward-biased. This shorts the LC circuit and stops the oscillation.

Because of the long time constant L/r of the coil, the current through the deflection coil does not rapidly decrease to zero. Instead it decreases gradually and linearly until it becomes zero at t5. Right after t5, a positive triggering voltage is supplied to the base of the transistor and the cycle described above is repeated.

The current flowing through the deflection coil during the trace period is composite, consisting of the current through the transistor and the damper diode.

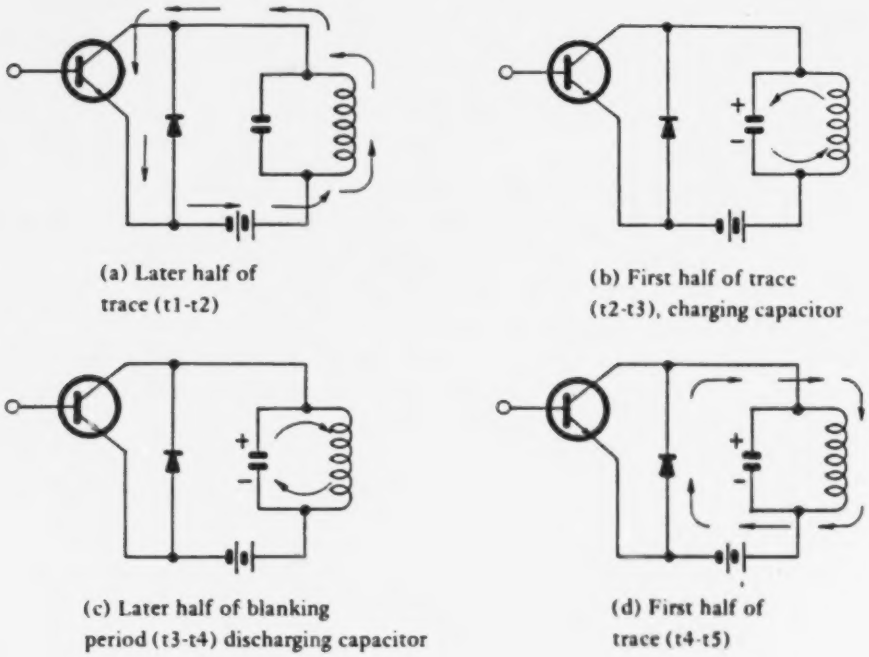
The wave-form of the current through the deflection coil during the entire cycle is shown in Figure 3-47(e). Figure 3-48 shows the direction of the current flow through the circuit during the entire cycle.

Horizontal output transistor and damper diode. A high-powered fast-switching transistor is used in the horizontal output transistor to handle the high flyback pulses safely and rapidly shift from saturation to cut-off. A heat sink is attached to the transistor, because heat dissipation is great.

The magnitude of the pulse voltage generated during the retrace period is approximately ten times more than the B+ supply voltage.

Since the B+ voltage is around 100 volts, the resulting pulse voltage is around 1,000 volts. Thus it requires a transistor with a handling voltage of more than 1,000 volts.

Similar characteristics with less internal resistance are required for the damper diode.



(a) Later half of trace (t1-t2)

(b) First half of trace (t2-t3), charging capacitor

(c) Later half of blanking period (t3-t4) discharging capacitor

(d) First half of trace (t4-t5)

Figure 3-48
Current flow in the deflection coil

Actual AFC and horizontal oscillator circuit

Figure 3-49 shows a horizontal oscillator circuit that uses a balanced AFC circuit as its phase detector. The AFC-control voltage is applied to the base of the oscillator transistor. A blocking oscillator circuit is used for the horizontal oscillator. The oscillation frequency is varied by adjusting the core of the horizontal oscillator transformer.

Actual horizontal drive and output circuit

Figure 3-50 shows a horizontal drive and output circuit. A low-impedance transformer is used to drive the horizontal output transistor. It allows sufficient base current.

The coil placed in series at the base circuit of the output transistor will increase the cut-off speed of the collector current. A pincushion adjustment transformer and linearity improvement capacitor are connected in series to the deflection coil. The function of this circuit is explained in the section on "Pincushion Circuits."

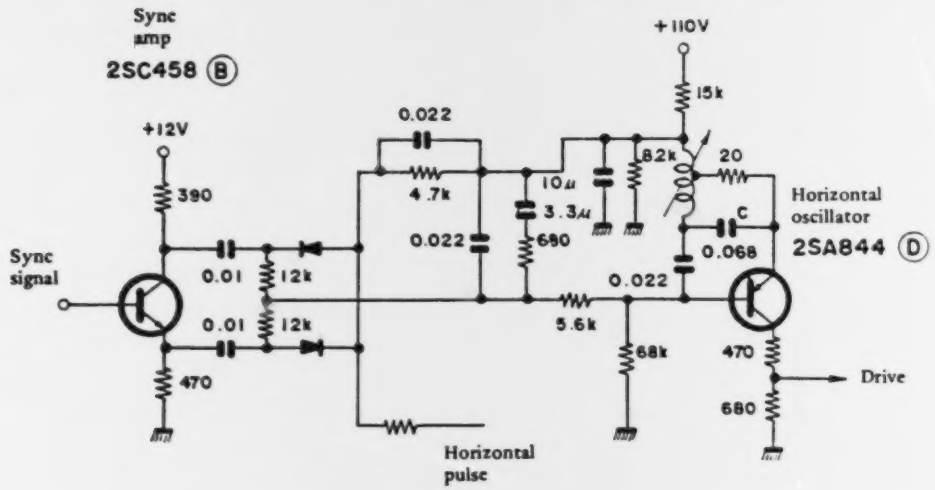


Figure 3-49
An AFC and horizontal oscillator circuit

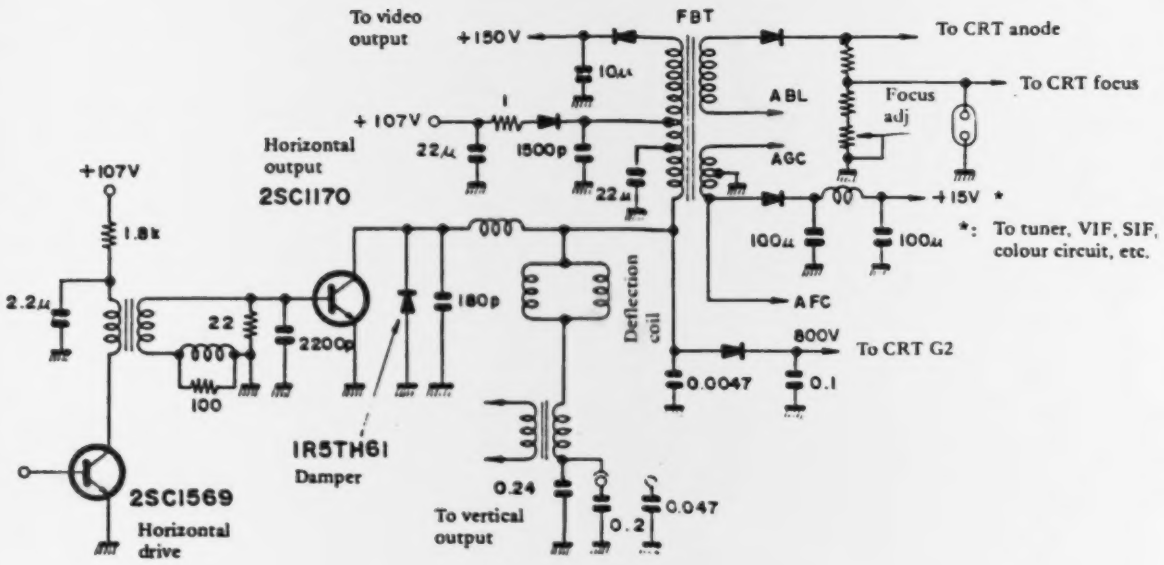


Figure 3-50
A horizontal drive and horizontal output circuit

Surrounding circuits of the horizontal deflection circuits

High-voltage generator circuit

A high voltage of around 25 kV is supplied to the anode of the colour CRT. The high voltage is generated by the horizontal output transformer (HOT) or flyback transformer (FBT), which is connected to the horizontal output transistor, as shown in Figure 3-51.

The flyback pulses from the HOT generated during the retrace periods are rectified by the high-voltage rectifier diode and supplied to the anode.

There are three kinds of rectifier circuits: the half-wave rectifier, the voltage doubler and the voltage tripler circuit.

The half-wave rectifier circuit is shown in Figure 3-51; the voltage doubler and tripler circuits are shown in Figures 3-52 (a) and (b).

The magnitude of the flyback pulses generated during the retrace period is around 1 KV.

If the half-wave rectifier circuit is used, the winding ratio of the HOT must be high; thus the size of the transformer becomes big. But if the voltage doubler or tripler circuit is used, the winding ratio and the size of the HOT can be made smaller.

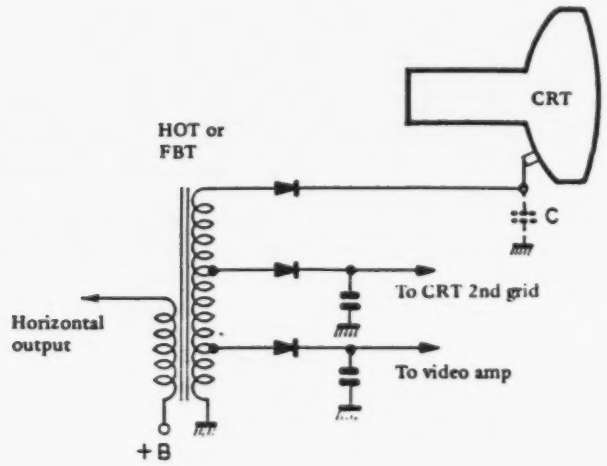
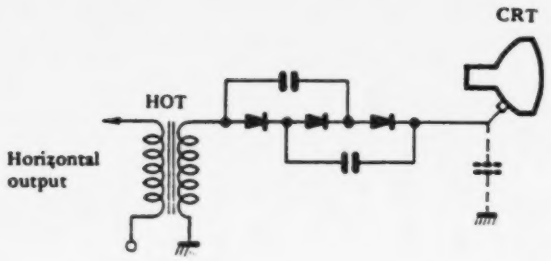


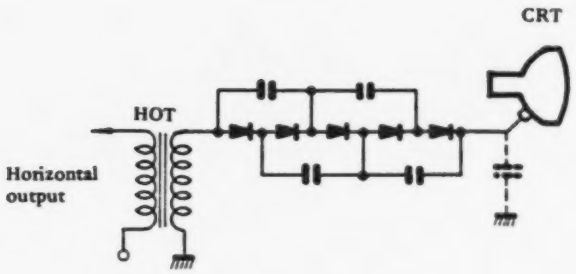
Figure 3-51
High-voltage generator circuit (half-wave rectifier)

Figure 3-53(a) shows the principle of the voltage doubler circuit.

When the pulse voltage e1 [Figure 3-53(b)] is applied, C1 is charged up to the level of e1 by the current flow indicated by the dashed curve (1). When e2 is applied, D2 conducts and capacitor C2 is charged by the current flow indicated by the dashed curve (2). C2 is charged by e2 plus the voltage stored across C1 which is e1. Thus the voltage charged across C2 is equal to e1 + e2.

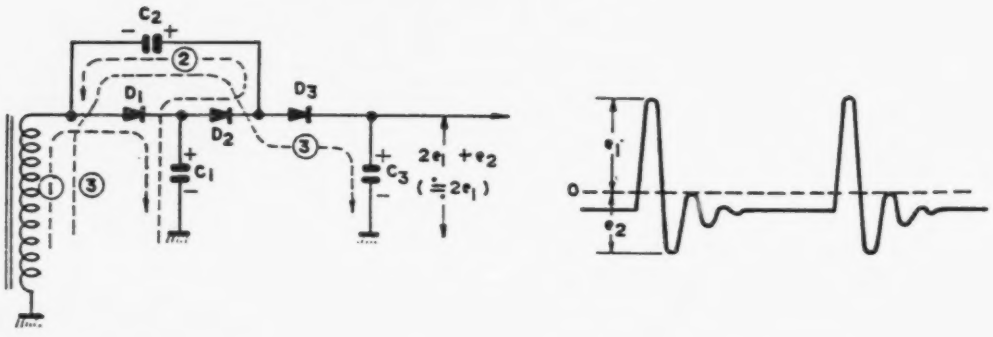


(a) Voltage doubler



(b) Voltage tripler

Figure 3-52
High-voltage generator circuits



(a) Basic circuit

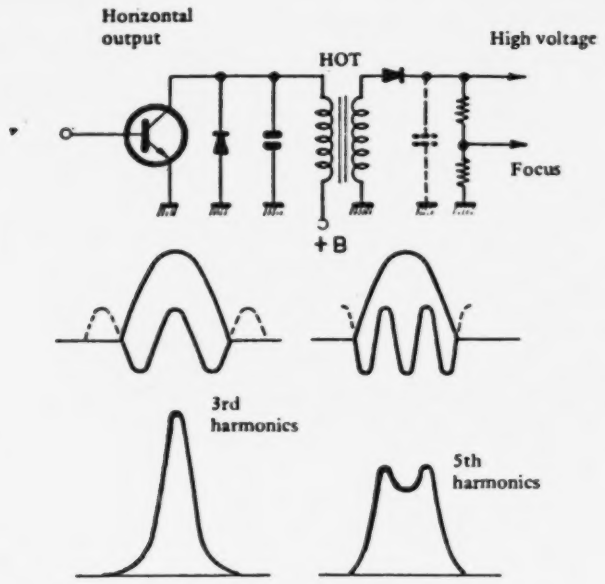
(b) Wave-form at HOT

Figure 3-53
Voltage doubler in a high-voltage circuit

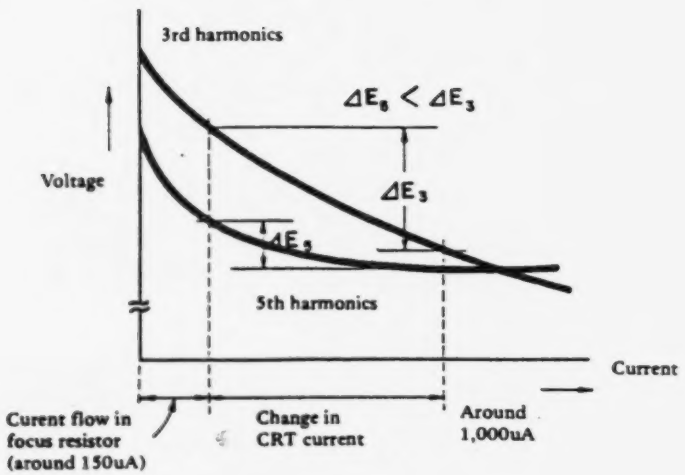
When another positive pulse e1 is applied to the circuit, D3 conducts and the voltage (e1 + e2) + e1 = 2e1 + e2 appears across C3. This circuit originally works as a voltage tripler circuit for a sine wave input. But since the level of e2 is much smaller than e1, the circuit is considered a voltage doubler rectifier circuit.

Figure 3-52(b) shows a voltage tripler rectifier circuit. This is actually a

doubler circuit with an additional rectifier circuit set. If the input to the circuit is a sine wave, the output becomes five times that of the original voltage.



(a) Wave-form at secondary of horizontal output transformer



(b) High-voltage stabilisation

Figure 3-54
High-voltage stabilising circuit

High-voltage stabilisation

Because of a large beam current value and the reproduction of DC components of the image in colour CRT circuits, the average of the beam current value in the colour CRT varies considerably as the image on the screen changes.

The high voltage of the colour CRT is generated by the flyback pulses. But this voltage generation has poor regulation, which causes changes in the size of the raster, poor convergence and poor focus, and affects the other circuits using the flyback pulses as a power-supply voltage.

Figure 3-54(a) shows a high-voltage stabilising circuit. This circuit uses no control circuit, but the HOT is tuned to the harmonics of the flyback pulses. The HOT is tuned to the third and fifth harmonics.

If the HOT is tuned to the fifth harmonics, the peak of the pulse at its secondary is wider, as shown in Figure 3-54(a). Therefore the conduction angle of the rectifier becomes wider and the stability of the high-voltage supply is improved.

Focus circuit

There are two kinds of focus circuits commonly used in colour CRT circuits. They are the low-voltage static focusing circuit (LV type) and the high-voltage static focusing circuit (HV type).

The LV type is usually used for small-sized colour CRTs (less than 20 inches) where the screen grid voltage is used for the focus voltage of the CRT.

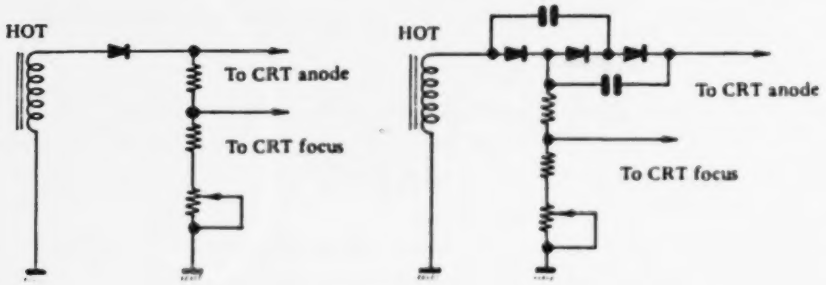


Figure 3-55
A focus circuit

In the HV type the focus voltage is around 16 per cent to 20 per cent of the anode voltage. The focus voltage must be able to follow the change in the anode voltage as fast as possible.

Figure 3-55 shows a focus circuit.

Medium- and low-voltage power-supply circuit

Various power-supply circuits are connected to the HOT circuit, as shown in Figure 3-56.

The type of circuits connected varies with its corresponding load. For

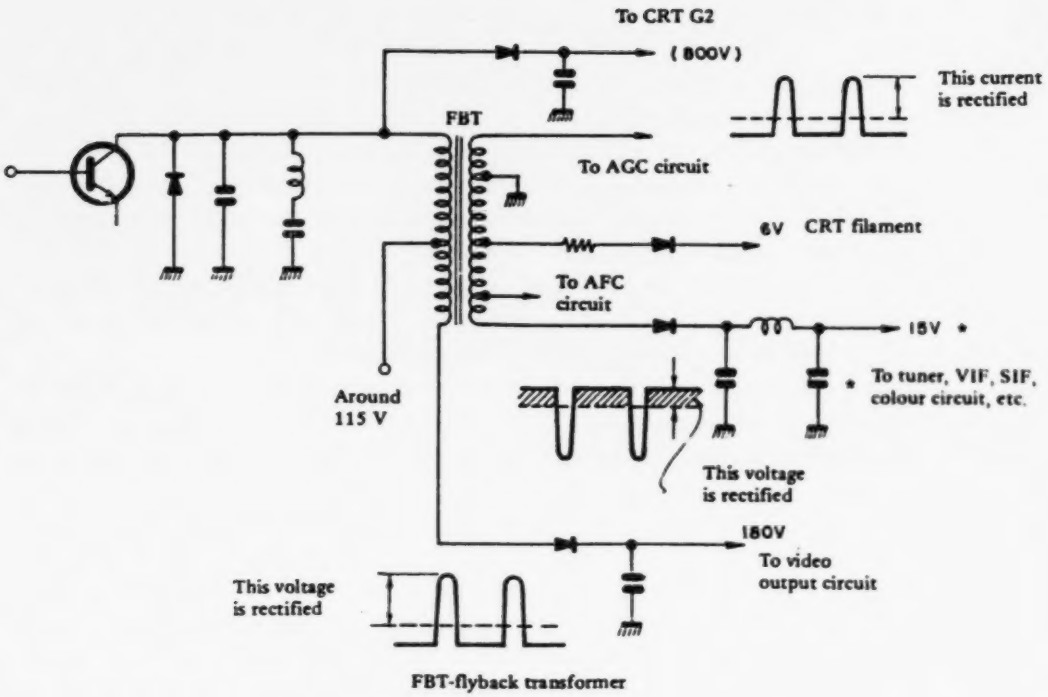


Figure 3-56
Medium- and low-voltage power-supply circuit

instance, for a load like the CRT screen which requires a considerably high voltage but a small current, flyback pulses are used. For a load like the filament of the CRT which requires a low voltage but a high current supply, the supply is taken from the secondary of the HOT.

The secondary winding of the HOT generates reverse polarity pulses during the trace or scanning period. These pulses are rectified and used for the filament voltage and for circuits requiring low-voltage supply.

Since these rectified pulses are wide, they are not significantly affected by the change in the high and AC voltage and thus provide a relatively stable low-voltage supply.

Pincushion circuits

The screen of the CRT is a curved surface which is not symmetrical to the deflection centre. The distance between the deflection centre and the screen is greater at the corners of the screen.

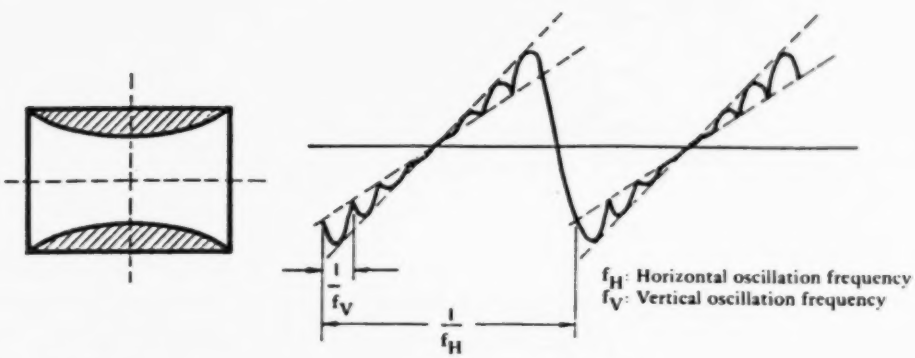
As the beam is deflected linearly towards the corners of the screen, the distance it travels from the gun to the screen increases. This results in the beam's being deflected more at the corners. Thus a spool-shaped raster is produced. This distortion, called pincushion distortion, is greater in wide-deflection angle CRTs.

To compensate for the distortion of the raster, the current through the deflection coils must be controlled as the beam is deflected. This is done by the pinchusion-control circuit of the horizontal and vertical deflection circuits.

Vertical pincushion circuit

In Figure 3-57(a) vertical pincushion distortion can be attributed to insufficient deflection at the upper and lower edges of the screen. To eliminate the distortion, a tolerance or compensating current has to be supplied to the vertical deflection coil.

Owing to the physical structure of the CRT, the distortion at the edges is parabolic. This parabolic distortion is compensated by adding a parabolic current to the vertical deflection current as in (b).



(a) Upper and lower pincushion distortion

(b) Current needed for compensation

Figure 3-57
Compensation of upper and lower pincushion distortion

The frequency of the compensating current should be equal and in phase with the horizontal deflection current. Furthermore, the amplitude of the parabolic current should be greater when the beam is deflected at the upper and lower edges of the screen.

A saturation reactor, shown in Figure 3-58(b), is used to generate the parabolic current. Figure 3-58(a) shows a typical vertical pincushion circuit. For CRTs with a deflection angle of less than 90 degrees, the vertical pincushion distortion is minimal. Thus, instead of using a pincushion tolerance circuit, the winding of the vertical deflection coil is designed to compensate the vertical pincushion distortion.

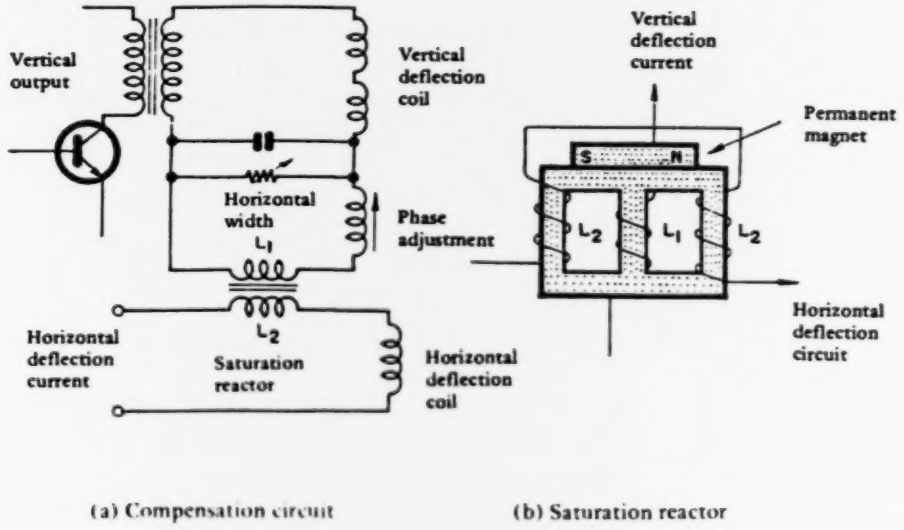


Figure 3-58
Compensation circuit for upper and lower pincushion distortion

Horizontal pincushion circuit

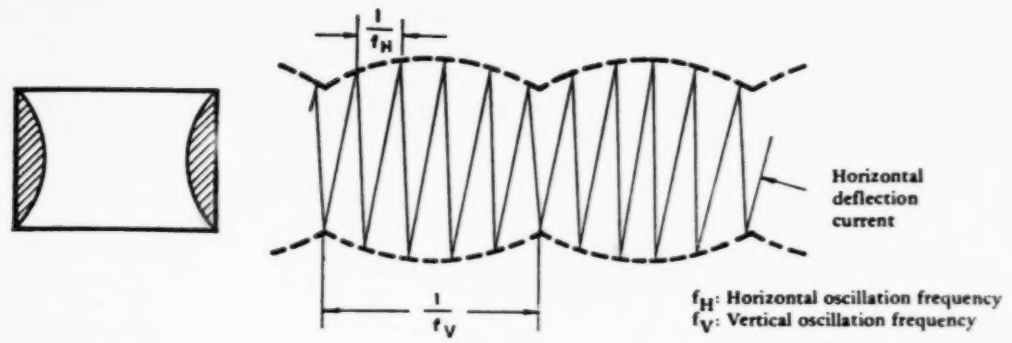
Figure 3-59(a) shows horizontal pincushion distortion, which can be attributed to insufficient deflection at both sides of the screen. This distortion is eliminated by modulating the horizontal deflection current with a compensating current.

A parabolic current with a frequency and phase equal to the vertical deflection current is used to modulate the amplitude of the horizontal deflection current. The resulting horizontal deflection current is shown in Figure (b).

The circuit in Figure 3-60(a) is used to generate the compensating current. It uses a saturation reactor in (b).

The inductance of the reactor decreases when the compensating current (current through L1) increases and it increases when the compensating current decreases.

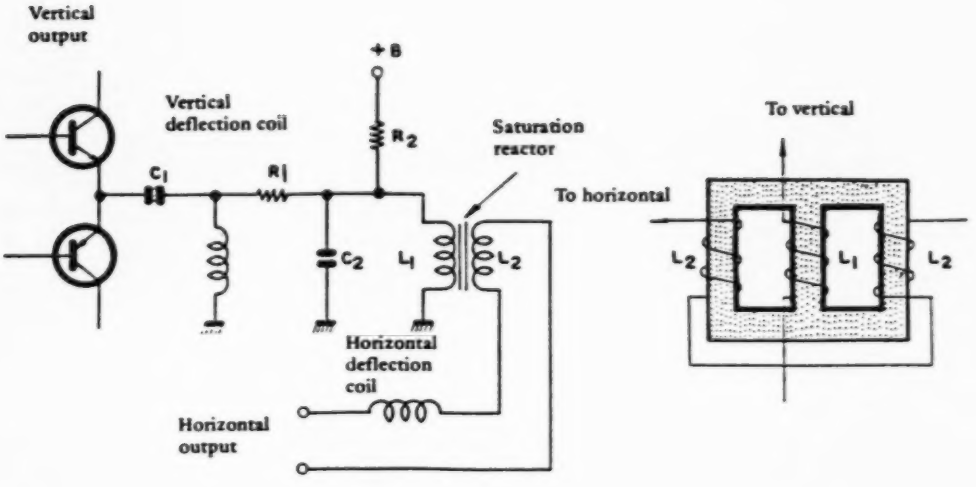
The parabolic current from the integrator circuit formed by R1 and C2 is supplied to L1. This produces a parabolically amplitude-modulated horizontal current through the horizontal deflection coil, which eliminates the horizontal pincushion distortion.



(a) Right and left pincushion distortion

(b) Compensation current

Figure 3-59
Compensation of right and left pincushion distortion



(a) Compensation circuit

(b) Saturation reactor

Figure 3-60
Compensation circuit for right and left pincushion distortion

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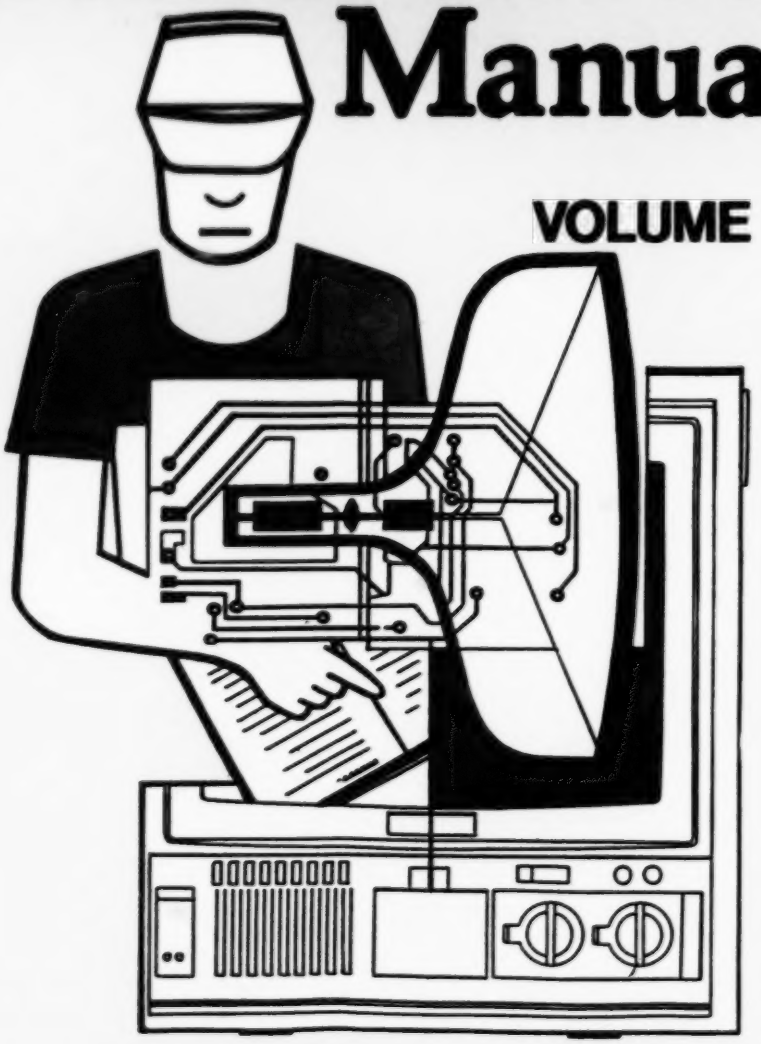

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VOLUME 8

BY MASAAKI MUKAI AND RYOZO KOBAYASHI

Part 3: Synchronisation and deflection circuits (Instructor's manual)

ASIAN AND PACIFIC SKILL DEVELOPMENT PROGRAMME
INTERNATIONAL LABOUR OFFICE
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Part 3: Synchronisation and deflection circuits

Principle of synchronised deflection

The deflection of the modulated electron beam must be synchronised with the image to be reproduced. The beam must be deflected in successive order from left to right and from top to bottom. Furthermore, deflection must be timed so that the picture elements are assembled in the same way the camera at the transmitter disassembles the image to be transmitted. The timing of horizontal and vertical deflection is called synchronisation.

There are two methods of deflection: static and electromagnetic. Permanent magnets are used in static deflection while electromagnetic coils are used in electromagnetic deflection. Electromagnetic deflection is used in TV receivers. Sawtooth currents are supplied to the deflection coils to produce an electromagnetic field needed to deflect a beam. The frequencies of the currents for horizontal and vertical deflection coils are 15,750 Hz and 60 Hz, respectively.

The deflection of the beam or the scanning of the CRT is synchronised with the scannning of the camera at the transmitter by sync signals transmitted with the video signal. Figure 3-1 shows a block diagram of the deflection circuits.

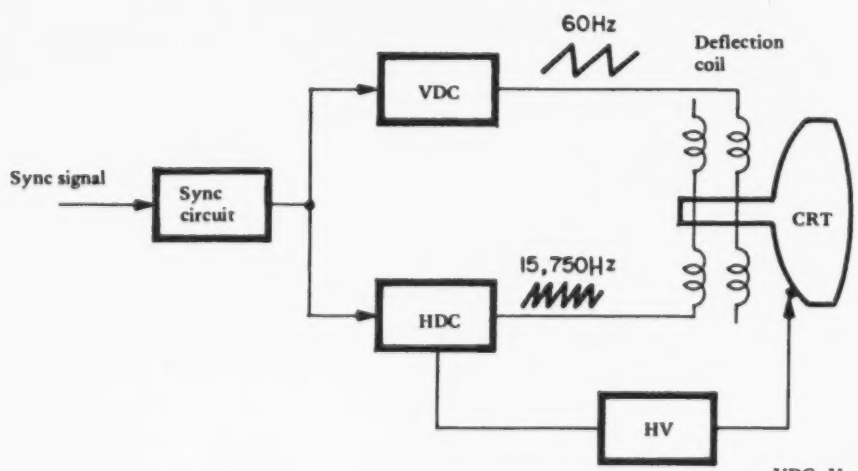


Figure 3-1
Functional block diagram of synchronisation and deflection circuits

Electron beam deflection

Figure 3-2 illustrates the principle of static deflection. The magnitude and direction of the beam's deflection depend on the strength and direction of the magnetic field. The direction of the beam can be determined using Flemming's left-hand rule as illustrated in Figure 3-3. Examples of the direction of the beam's deflection and the corresponding direction of the magnetic fields are shown in Figure 3-2.

CRTs in television receivers use a pair of coils for deflecting the beam. These are horizontal and vertical deflection coils. Each sawtooth current flowing through the coils produces varying electromagnetic fields which deflect the beam all over the screen.

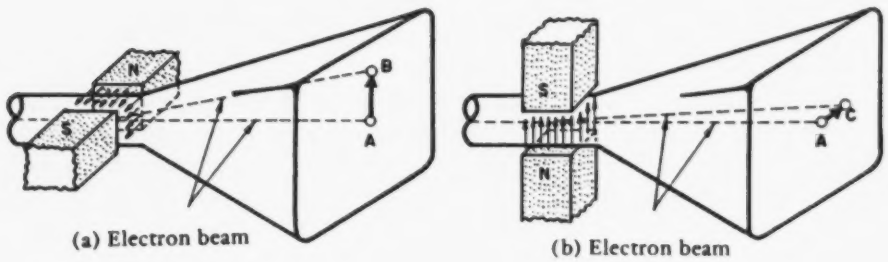


Figure 3-2
Principle of static deflection

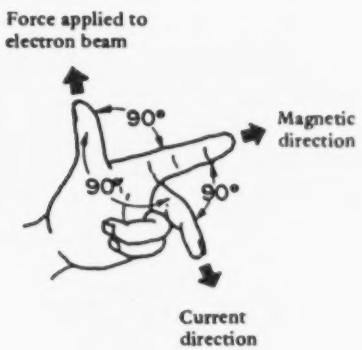


Figure 3-3
Flemming's left-hand rule

Magnitude of deflection (electromagnetic deflection)

Magnitude of deflection can be obtained by referring to Figure 3.1. Magnitude of deflection is proportional to the strength of the magnetic field and inversely

proportional to the square root of the anode voltage. Assuming some of the parameters are constant, the strength of the magnetic field should vary linearly for linear deflection. Also note that if the anode voltage is increased, the strength of the magnetic field should be increased to get the same magnitude of deflection.

The strength of the magnetic field (H) produced by the deflection coils is proportional to the product of the number of turns of the coils (N) and the current (I) flowing through them. Thus a greater value of NI means a stronger magnetic field and a larger deflection.

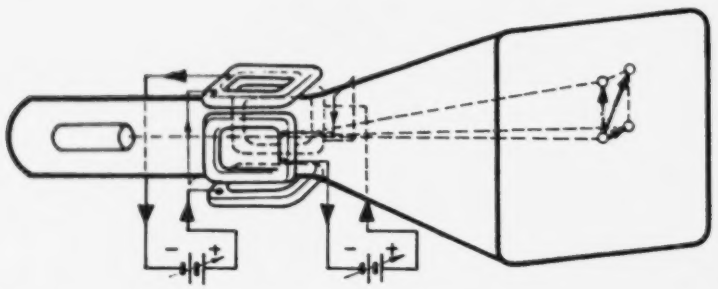


Figure 3-4
Deflection of electron beam

Sawtooth wave

Linear scanning of the CRT is achieved only if the electron beam is deflected linearly. This requires the current through the coils to be a linear sawtooth wave. Figure 3-6(a) shows an ideal linear sawtooth wave. The wave can be divided into two sections: a) linear increase from its minimum to its maximum value and b) instantaneous drop from its maximum to its minimum value.

However, it is impossible to generate an ideal sawtooth wave because zero decay time is just not possible. An actual sawtooth wave is shown in Figure 3-6(b). Similarly, this wave can be divided into two sections: a) interval of the linear increase from its minimum to its maximum value (Tt, trace period) and b) interval of the sudden decrease from its maximum to its minimum value (Tr, retrace period).

Sawtooth generator circuit

Figure 3-7 shows the principle for generating a sawtooth wave. A sawtooth wave is generated by constantly charging and discharging a capacitor.

The circuit in Figure 3-7(a) will be used as an example to explain how a sawtooth wave is generated. Assume that capacitor C has no initial stored charges. When switch S is on, the supply voltage E_b charges C through resistor R. The voltage across C increases until it equals the supply voltage. If S is switched off after C is fully charged, C immediately discharges. By constantly switching S on and off, a sawooth wave is generated, as shown in Figure 3-7(b). The shape

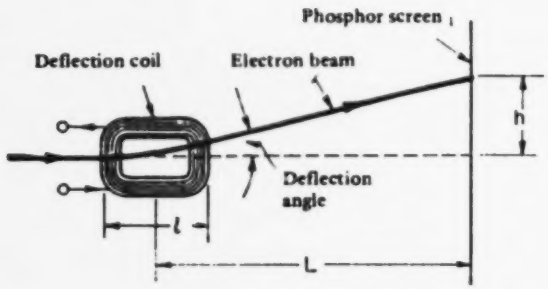
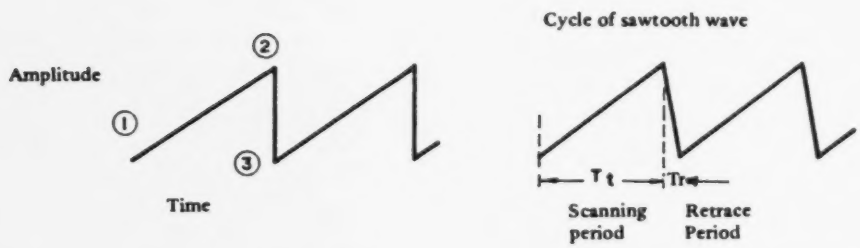


Figure 3-5
Magnitude of electromagnetically deflected electron beam



(a) Ideal sawtooth wave

(b) Sawtooth wave actually used

Figure 3-6
Sawtooth wave

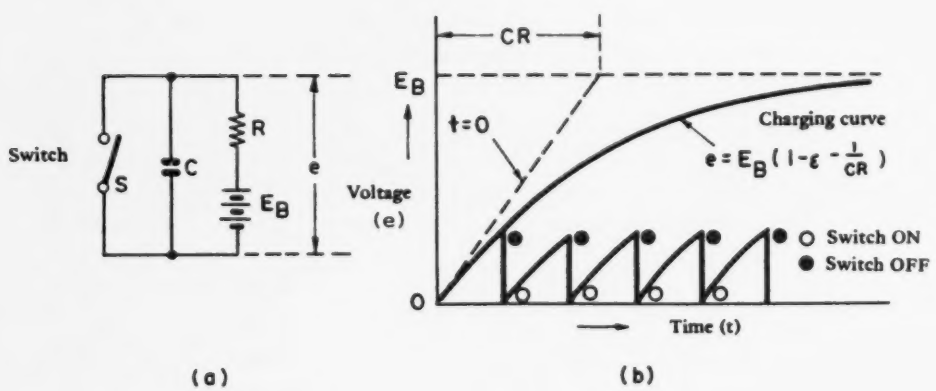
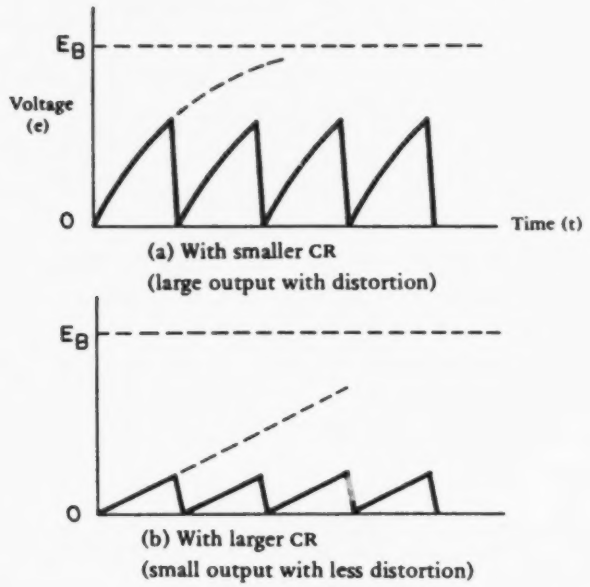


Figure 3-7
Basic sawtooth-wave generator circuit

of the sawtooth wave depends on time constant CR. The larger the CR, the longer it takes to charge C. Assuming a constant cycle in the switching on and off of S, the generated sawtooth wave has better linearity if CR is set to a larger value, as shown in Figure 3-8. If capacitance is expressed in uF and resistance in Mohms, the dimension of CR will be in seconds. Sawtooth waves generated at two different time constants are also shown in Figure 3-8.

Figure 3-9(a) shows a fundamental sawtooth-wave generator circuit. A transistor is used as a switch. The transistor is switched on during the interval when positive pulses are applied to the base, and is off between intervals of the pulses. The circuit shown in Figure 3-9(b) is just an equivalent of Figure 3-8(a).

Figure 3 8
Sawtooth wave and time constant (CR)



(a) With smaller CR
(large output with distortion)

(b) With larger CR
(small output with less distortion)

During the trace period Tt, the transistor is off and the supply voltage Vcc charges C at a rate set by CR. During the retrace period Tr when the positive pulses are applied to the base, the transistor is on. In this case, C discharges through the transistor at a rate set by time constant CRc. Rc is the internal resistance of the transistor which is negligible compared with R. Since Rc is very small, C discharges at a much shorter time than the time it charges. The slow increase in the voltage across C and the sudden decrease to its minimum value when it reaches its maximum forms a sawtooth wave, as shown in Figure 3-9(c).

The transistor used in the sample circuit is an NPN type. A PNP transistor could have also been used, but polarity of the keying pulses should be reversed. For this case, polarity of the sawtooth wave is also reversed.

Deflection coil

The deflection yoke mounted at the neck of the CRT consists of a pair of horizontal and vertical deflection coils. The current through each of these coils pro-

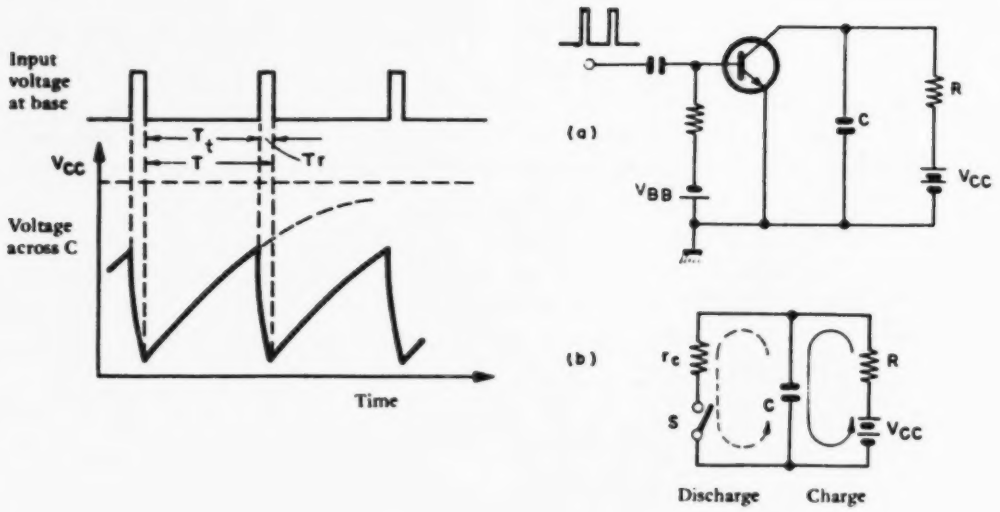


Figure 3-9
Sawtooth-wave voltage-generator circuit

duces a magnetic field which deflects the beam from left to right and from top to bottom.

There are various kinds of deflection coils. Picture 3-1 shows one example. For delta gun CRTs, the winding of the deflection coil is designed to produce a constant electromagnetic field. For in-line gun CRTs, the winding is designed to produce a distorted electromagnetic field to enable easy convergence adjustments for the three electron beams.

Picture 3-1
A deflection coil

The power requirement of a deflection coil is proportional to the anode voltage and the square of the deflection angle. Therefore a deflection coil requires more power at higher anode voltages and greater deflection angles. This requirement, however, varies with each type of deflection coil. The power re-

quirement for a deflection coil is generally proportional to its diameter and inversely proportional to its length. Table 3-1 shows characteristics of different types of deflection coils.

Table 3-1
Characteristics of different types of deflection coils

Deflection angle (degrees)	*Type of winding*				*Inductance (mH)*		*DC resistance*	
	Electron gun	*CRT neck diameter*	*Horizontal*	*Vertical*	*Horizontal*	*Vertical*	*Horizontal*	*Vertical*
90	Delta	36.5	Saddle	Troidal	0.57	24	0.6	14
110	Delta	29.1	Saddle	Saddle	0.87	25	0.75	14
110	Delta	29.1	Precision Troidal	Presision Troidal	0.32	0.88	0.43	1.45
90	In-line	29.1	Precision Troidal	Precision Troidal	0.64	1.17	1.71	2.41
90	In-line	29.1	Saddle	Troidal	2.1	90	2.2	40

Synchronisation circuits

Function of the sync signal

Image reproduction on the CRT screen must be synchronised precisely with the disassembly of the image in the camera at the broadcast station.

Broadcast stations transmit vertical and horizontal sync signals with the luminance or video signal. The signals are processed by the sync circuits of the receiver for synchronisation. The sync pulses synchronise the frequency of beam deflection in the CRT with the scanning frequency of the camera at the broadcast station. Thus the frequency of the sawtooth current through the horizontal and vertical deflection coils is equal to the frequency of the horizontal and vertical sync signals, respectively.

If the vertical deflection frequency (vertical oscillation frequency) is not equal to that of the vertical sync signal, the image reproduced on the screen rolls. If the horizontal deflection frequency is not equal to that of the horizontal sync signal, the image on the screen tears diagonally.

The vertical and horizontal deflection signals must also be in phase with their corresponding sync signals. The image on the screen will shift even if it is stable (does not roll or tear) if the sync signals and the deflection signals are equal in frequencies but out of phase. Figures 3-10(a) and (b) show shifting of the image when the vertical and horizontal deflection signals are not in phase with their corresponding sync signals.

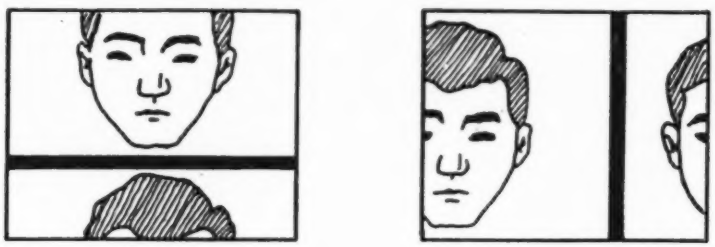


Figure 3-10
Phase relation of sync signals affecting reproduction of picture

Sync signals are multiplexed and transmitted with the luminance signal. The sync signals must be separated from the composite video signal before being supplied to the sync circuits. This prevents noise in the video information from affecting synchronisation of the receiver. Sync separator circuits are used to separate the sync signals from the composite video signal. These sync signals are further separated into horizontal and vertical sync signals before they are finally supplied to their respective circuits.

In driving the CRT, there is no need to separate the luminance signal or video information from the sync signals. The sync signals are modulated at a darker level than the black level of the luminance signal. Furthermore, the sync signals are present only during the retrace periods when the luminance signal is absent. Thus the sync signals serve as blanking pulses for the CRT during the retrace periods and this does not affect image reproduction.

However, if the composite video signal is supplied to the sync circuits, the luminance signal can trigger the oscillator circuits and affect synchronisation.

Amplitude separator circuit

This circuit is used in separating the sync signal from the composite video signal.

Figure 3-11 shows a basic amplitude separator circuit. The composite video signal with negative polarity is coupled to the base of the separator transistor by C1. Time constant R1C1 is set to a large value. The circuit is biased so that only the sync signal triggers the transistor. Thus, only the sync signals are amplified and taken at the output.

Let us see how the circuit works. During the retrace period, the sync pulse decreases the base voltage of the transistor and turns it on. Base current flows, charging the capacitor with the polarity indicated in the figure. Collector current also flows, producing an amplified sync signal at the output. At the start of the trace period, C1 starts to discharge through R1. The polarity of the voltage across R1 due to the discharge is such that the base is positive with respect to the emitter. This turns off the transistor. Since the transistor does not conduct, the luminance signal during the trace period is not amplified. C1R1 is set to a large value to get a long discharge time. This keeps the transistor cut off during the trace period. When the next sync pulse is supplied, the transistor turns on again, repeating the cycle. Therefore the output of the circuit consists only of the sync (horizontal and vertical) signals.

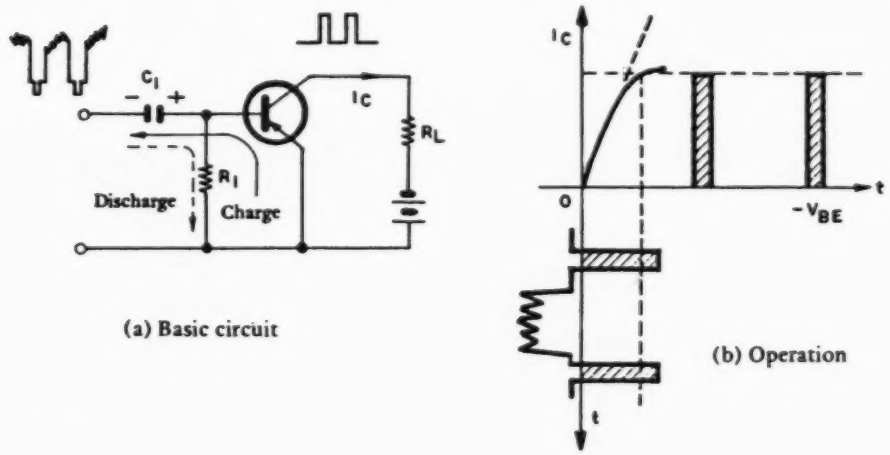


Figure 3-11
Sync separator circuit

In an NPN transistor the polarity of the composite video signal supplied to the base should be positive. In this case negative sync signals are taken at the output.

A switching transistor with good saturation response and a small driving voltage requirement is used. This makes it possible to supply the composite video signal (around 1 Vp-p) from the video-detector output to the separator circuit and get undistorted sync signals at the separator output circuit.

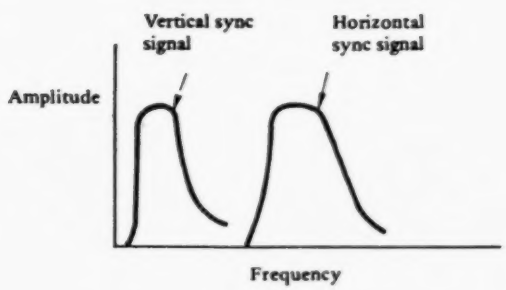
Frequency separator circuit

The signal separated by the amplitude separator circuit consists of horizontal and vertical sync signals. These signals have to be further separated before they are supplied to the horizontal AFC and vertical oscillator circuits, respectively. The horizontal signal is a high-frequency signal consisting of narrow pulses; the vertical signal is a low-frequency signal consisting of wide pulses.

Figure 3-12 shows the frequency spectrum of the horizontal and vertical sync signals. These signals are separated from each other by the frequency separator circuit. The vertical signal is taken from a low-pass filter; the horizontal signal, from a high-pass filter.

Figures 3-13(a) and (b) show basic low- and high-pass filter circuits used in frequency separator circuits. The low-pass filter in (a) is called an integrator, since the output is integral to the input. The high-pass filter in (b) is called a differentiator, since its output derives from the input.

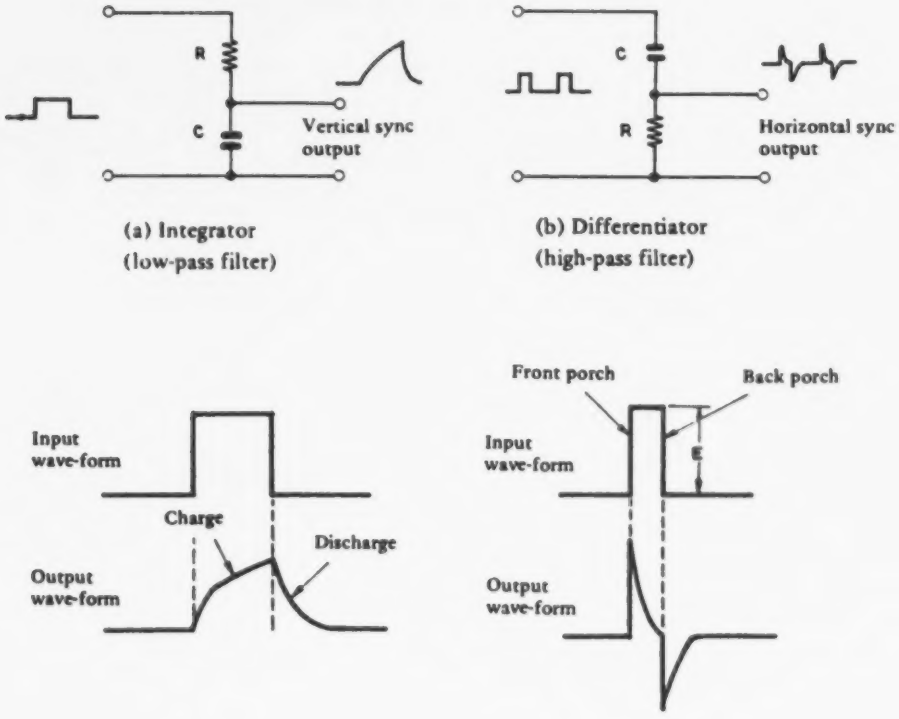
Figure 3-12
Frequency spectrum of horizontal and vertical sync signals



Integrator circuit. During the pulse periods the voltage across capacitor C increases rapidly from its initial value to its maximum value, which is equal to the peak of the pulse signal. The rate of increase in voltage across C is determined by time constant CR. During the interval between the pulse signals, C discharges. Figure 3-13(b) shows the input and the corresponding output of the integrator circuit shown in (a).

Since the duration of the vertical pulses is much longer than that of the horizontal pulses, the charged voltage across C due to the horizontal pulses is negligible compared with voltage due to the vertical pulses.

Figure 3-13
Frequency separator circuits



Thus, when the sync signals are supplied to the input, the output is mainly due to the vertical pulses. A simple way to look at it is to consider the frequency response of the circuit. Since the integrator is a low-pass filter, the vertical signal with low frequency is passed, while the horizontal signal with high frequency is bypassed. Figure 3-14(a) shows the input and the output signals of the integrator circuit.

Two to three stages of integrator circuits are used to filter the horizontal from the vertical sync pulses. This attenuates the horizontal pulses, since their presence in the vertical sync circuits affects vertical synchronisation.

Differentiator circuit. The differentiator circuit shown in Figure 3-15(a) is similar to a CR coupling circuit. However, time constant CR of the circuit is comparatively small, usually around 0.8 to 1.0 usec.

When the horizontal sync pulse in (b) is applied, the capacitor is charged by the large current, which flows during the front porch of the pulse. Since time constant is 1 usec, the capacitor becomes fully charged in about 1.5 usec, long before the end of the 5 usec duration of the pulse. The voltage across capacitor C with respect to time is shown in (c). The curve in (d) is the voltage across resistor R, which is the difference between pulse and capacitor voltage. Since the

current through and the voltage across have the same wave-shape, the curve above zero level in (d) is also the charging current. After the duration of the pulse, C discharges through R. This discharge current is the curve below zero level in (d). It is negative, since the direction of the discharge current is opposite the direction of the charging current.

Figure 3-14
Input/output wave-form of the integrator and differentiator circuits

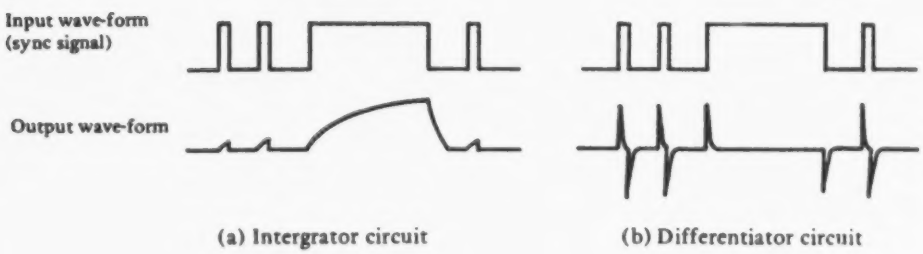
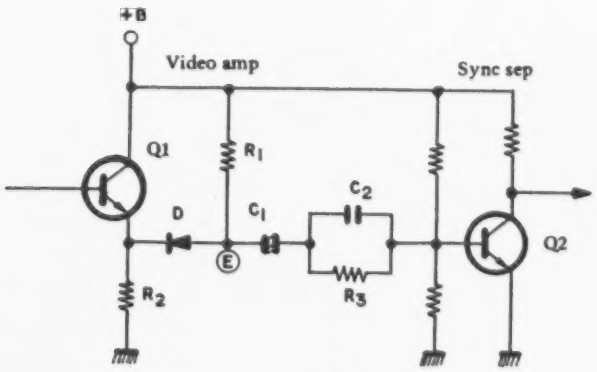


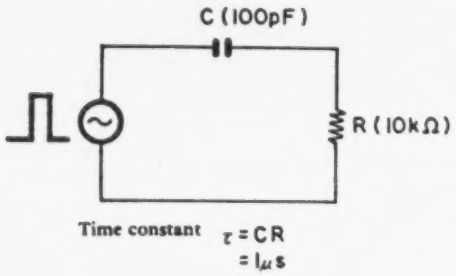
Figure 3-14 (b) shows sync signals applied to the differentiator circuit and the output. In actual sync circuits the average of the horizontal sync signals is used to control the horizontal oscillation frequency.

Noise-suppression circuit

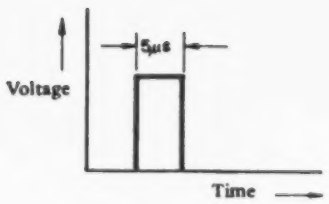
Noise pulses picked up during the transmission of the TV signal greatly affect synchronisation of the receiver. Noise in the composite video signal should be filtered before the signal is fed to the sync separator circuit. If noise is not filtered, it is also taken by the sync separator circuits and supplied to the sync circuits. Noise triggers the oscillators and disrupts synchronisation. A noise-suppression circuit is used to filter unwanted noise. Examples of noise-suppression circuits are shown in Figures 3-16 and 17.

Figure 3-16
Noise-suppression circuit

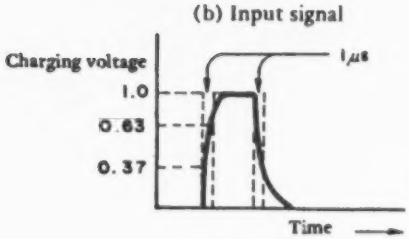




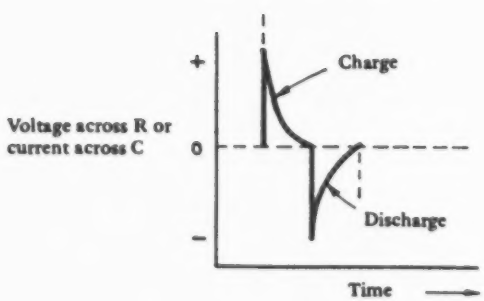
(a) Differentiator



(b) Input signal



(c) Voltage across C



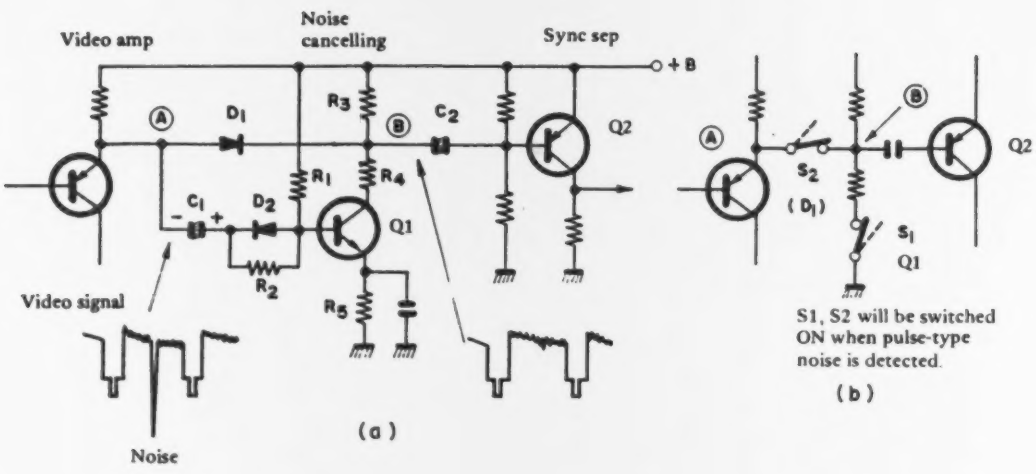
(d) Current flow in the circuit

Figure 3-15
Differentiator circuit

The noise-suppression circuit in Figure 3-16 is formed by C2, R3 and D, which is a noise-clipping diode. Positive composite video signals from the emitter of Q1 are supplied to the cathode of the diode. The noise-clipping diode is forward-biased by R1 and R2, so the diode remains on during the sync pulses. However, noise in the composite video signal drives the cathode to a potential higher than the potential at (E), which reverse-biases the diode. Therefore, noise is clipped and not supplied to the sync separator transistor Q2.

C1 is made much larger than C2 to make time constant C2R2 small. This makes the voltage across C1 due to noise negligible compared with the voltage across C2. Thus the bias voltage of the sync separator transistor Q2 is not altered significantly, so Q2 remains within the proper operating regions and functions steadily.

Figure 3-17
Noise-suppression circuit



In Figure 3-17, Q1 and D1 are cut off by noise. Thus, noise is filtered from the composite video signal supplied to the sync separator circuit. In the absence of noise, R1 forward-biases the base-emitter junction of Q1, turning it on. When Q1 is on, it conducts such that the voltage at (B) is lower than the voltage at (A). D1 becomes forward-biased and couples the composite video signal to the sync separator circuit. C1 biases D2 such that D2 is not forward-biased by sync signals. This keeps Q1 on. When noise with a level more negative than the sync signals appears, D2 conducts. Thus, noise is coupled to the base of Q1 and reverse-biases the base-emitter junction. Q1 is turned off and stops conducting. When this happens the voltage at (B) becomes higher than the voltage at (A). D1 becomes reverse-biased and does not couple the noise to the input circuit of the sync separator transistor circuit.

Actual sync circuit used in TV receivers

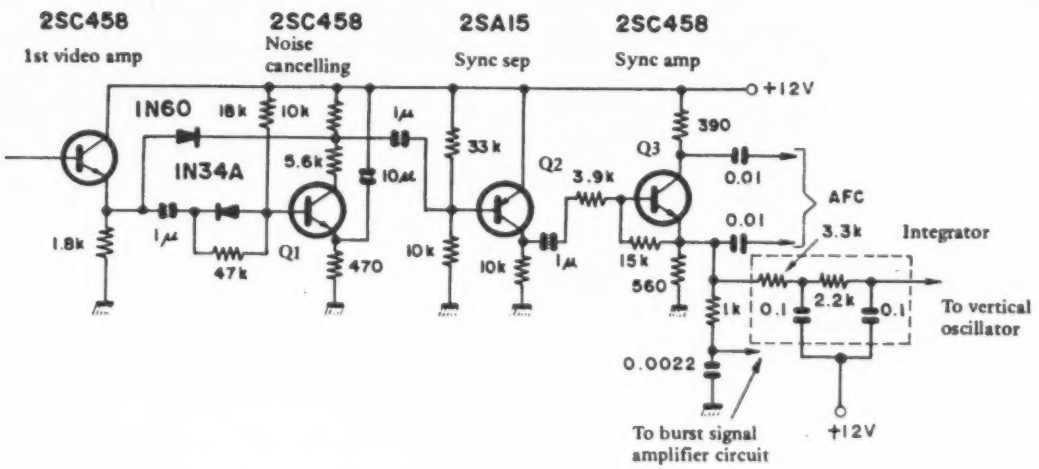
Figure 3-18 shows an actual sync circuit. The sync separator circuit is usually

connected to the emitter circuit of the video amplifier transistor (emitter-follower) for matching purposes. The low-output impedance of an emitter-follower circuit is needed to match the low-input impedance of the sync separator circuit during saturation.

In Figure 3-18 the noise-separator is connected before the sync separator and sync amplifier circuit. The sync amplifier performs phase-splitting, waveform sharpening and noise reduction. Positive and negative sync signals needed for the balanced AFC circuit are supplied by the sync amplifier circuit. Figure 3-19 shows a sync circuit using an IC. The IC functions as a) sync separator, b) noise suppressor, c) IF AGC, d) RF AGC, e) video amplifier and f) pulse amplifier.

The composite video signal taken from the video detector is fed to pin 10 and amplified by the video amplifier circuit. The noise-suppressor circuit filters noise in the composite video signal. Pin 14 supplies a composite video signal free of noise. This signal is coupled to pin 15 by C1 and R2. The output is taken from pin 16 and then fed to the horizontal AFC and integrator circuits.

Figure 3-18
A sync separator circuit



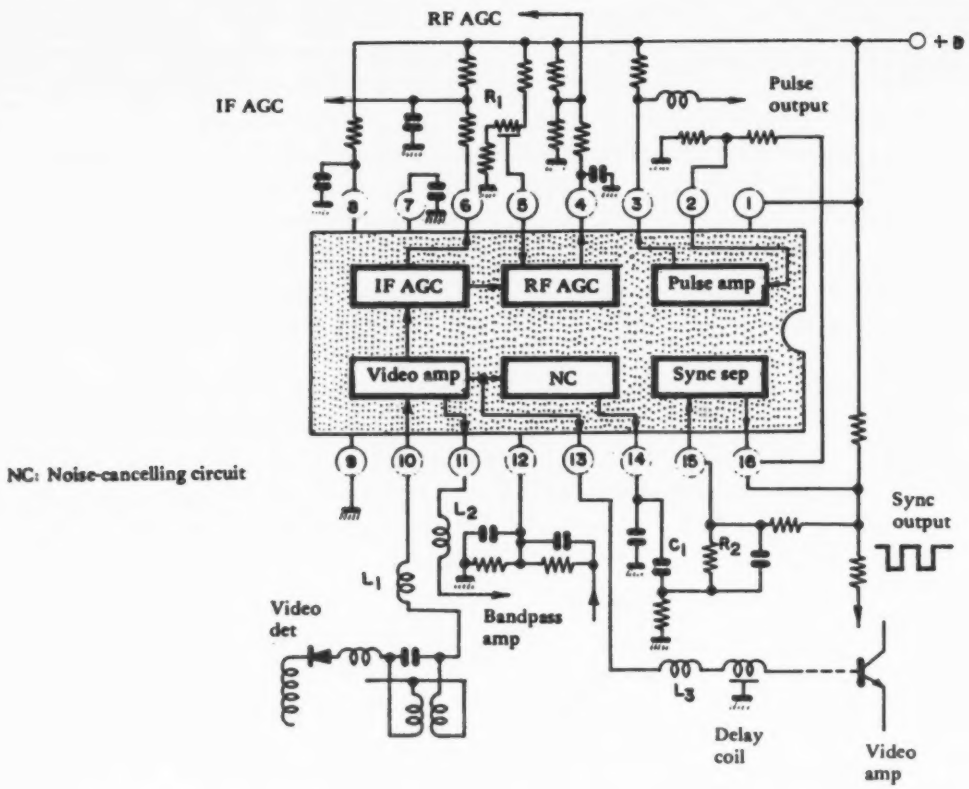


Figure 3-19
An IC sync separator circuit

Vertical deflection circuits (VDCs)

Block diagram of the VDC

Figure 3-20 shows a block diagram of the vertical deflection circuit (VDC), which consists of the vertical oscillator, vertical drive and the vertical output circuits. The vertical oscillator circuit generates a sawtooth voltage which is wave-shaped and amplified by the VDC. The vertical output circuit amplifies the voltage and supplies a sawtooth current to the vertical deflection coil. The frequency and phase of the vertical oscillator circuit are controlled by the vertical sync signal.

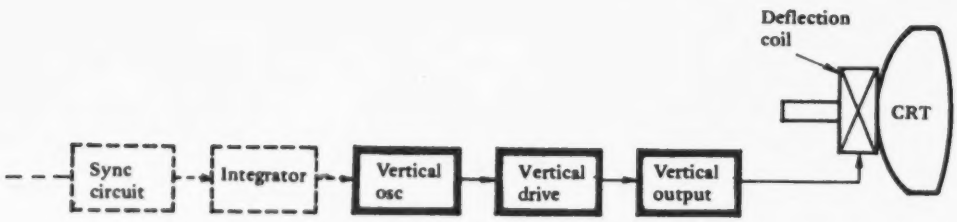


Figure 3-20
Functional block diagram of the vertical deflection circuit

Vertical oscillator circuit

A sawtooth voltage is usually generated by constantly charging and discharging a capacitor. The vertical oscillator transistor is used as a switch which determines the cycle of the charging and discharging of the capacitor. It operates in the cut-off and saturation regions only. Either a blocking oscillator or a multivibrator is used in the vertical oscillator circuit.

Blocking oscillator circuit. Figure 3-21(a) shows a blocking oscillator used in a sawtooth-voltage generator circuit. The base and the collector of the transistor Q are electromagnetically coupled by a blocking transformer. The sawtooth voltage is taken across R3.

When power is applied to the circuit, the voltage divider network formed by R1 and R2 + VR supplies a positive voltage to the base of Q. At this instant a large initial charging current flows through C and R3. This current makes the emitter voltage more positive than the base, keeping Q cut off. However, this current decreases as C is charged. As the current decreases, the emitter voltage also decreases. Figure 3-21(b) shows a plot of the emitter voltage with respect to time. When the emitter voltage becomes less than the base voltage, the transistor conducts and the collector current increases. Increase in collector current induces a voltage across L1, which in turn induces a voltage across L2. L2 is winded such that the polarity of this induced voltage tends to increase the base voltage. Increasing the base voltage increases the collector current, which in turn increases the induced voltage across L2 that tends to increase the base voltage. This is called positive feedback and continues until the transistor is saturated.

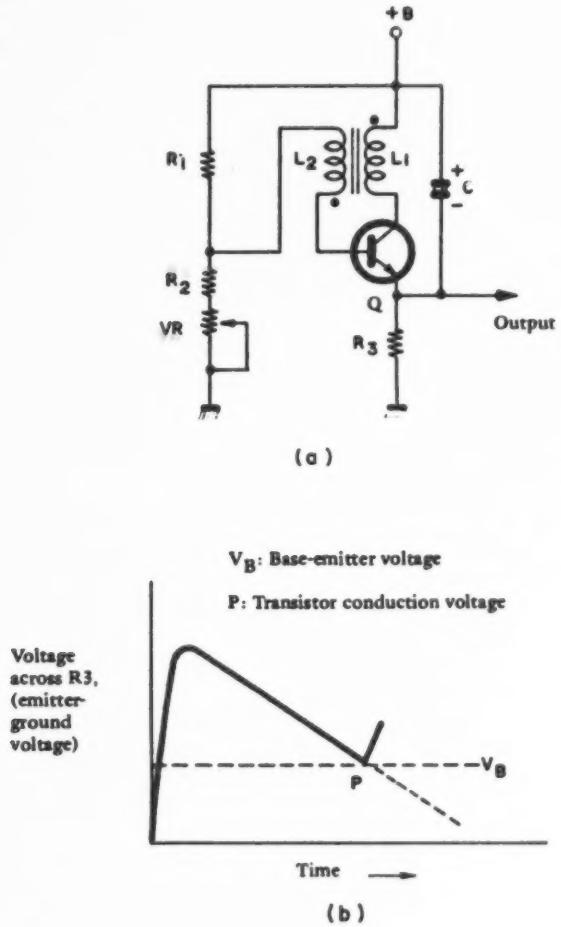


Figure 3-21
Blocking oscillator circuit used in a sawtooth generator circuit

During saturation the capacitor discharges through Q and R3. The change in collector current during saturation is negligible, keeping the collector current practically constant. When there is no change in the collector current, the induced voltage across L2 becomes zero and it decreases the base voltage to the DC base bias voltage. Decrease in the base voltage decreases the collector current and induces a voltage across L1, which in turn induces a voltage across L2. The polarity of the induced voltage this time tends to decrease the base voltage. Decreasing the base voltage lessens the collector current, which in turn increases the induced voltage that tends to decrease the base voltage. This is negative feedback. This continues until the transistor is driven to cut off.

The base voltage returns to its DC bias value. But the transistor remains cut off, since the capacitor starts to charge again, keeping the emitter more positive than the base. At this point the cycle is repeated.

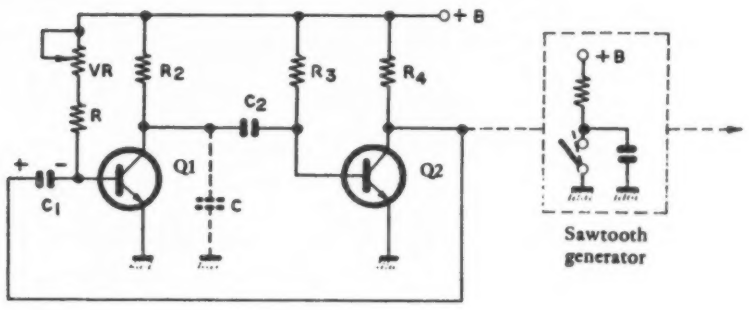
This cycle generates a sawtooth voltage across the R3. The frequency of this signal is controlled by time constant CR3. The linearity of the voltage depends much on the value of CR3. Thus the frequency of signal is varied by adjusting VR because the DC base voltage also affects the duration of the cycle.

Multivibrator circuit. Figure 3-22 shows another sawtooth-voltage generator circuit. Instead of a transformer, as in the blocking oscillator, it uses an amplifier circuit.

Q1 and Q2 are coupled by capacitors C1 and C2. When Q1 is on, its collector voltage turns off Q2. When Q2 is on, its collector voltage turns off Q1. The on-off period is determined by the time constant of the base circuit of each transistor.

The circuit enclosed by the broken line is the equivalent circuit of a sawtooth-voltage generator. To generate the sawtooth voltage, use the pulse signal generated at the collector circuit of the multivibrator transistor Q2 to switch on and off a sawtooth-voltage generator transistor or connect a capacitor at the collector circuit of Q1. In the latter, the sawtooth voltage is taken across C.

Figure 3-22
A multivibrator oscillator circuit



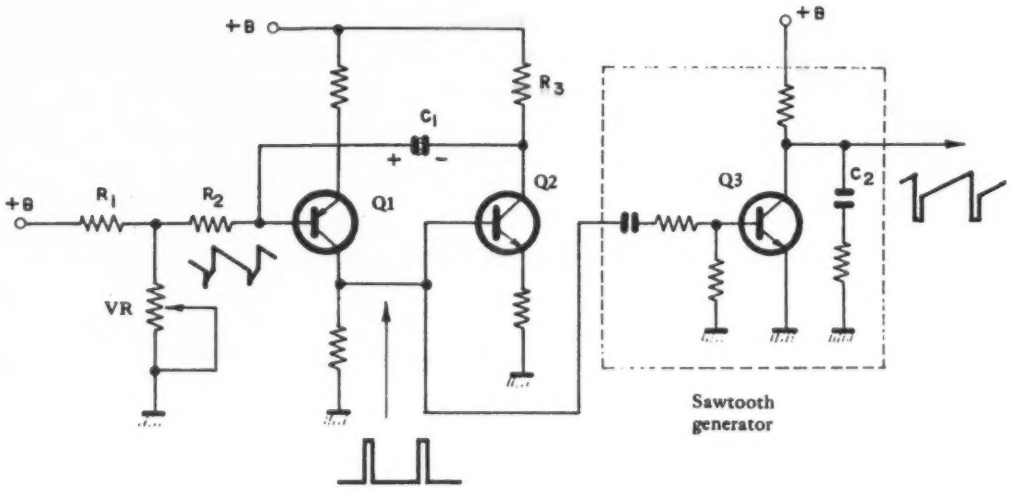
Other multivibrator circuits. Figure 3-23 shows another multivibrator used in a sawtooth-voltage generator circuit. This circuit uses a pair of PNP and NPN transistors. The collector of Q1 and the base of Q2 are coupled directly; the base of Q1 and the collector of Q2 are coupled capacitively.

When power is applied to the circuit, a positive voltage is supplied to the base of Q1 by the voltage divider network formed by R1 and VR. However, a more positive voltage supplied to the emitter drives Q1 into conduction. The collector voltage of Q1 increases as it starts to conduct. The increasing collector voltage of Q1 turns on Q2. When Q2 conducts, an increase in its collector current decreases its collector voltage due to the increase in the voltage drop across R3. Since C1 couples the collector of Q2 to the base of Q1, the base voltage of Q1 also decreases, making Q1 conduct more. As Q1 conducts more, the voltage of Q2 increases.

The two transistors are instantly saturated by this positive feedback. When

both are saturated, C1 is charged with the polarity shown in Figure 3-23. The voltage charged across C1 drives the base of Q1 positive. As C1 is charged, the base voltage increases until it exceeds the emitter voltage. When this happens, Q1 is driven to cut off. As it stops conducting, its collector current and voltage decrease. This turns off Q2.

Figure 3-23
A sawtooth generator circuit with multivibrator



When both transistors are off, C1 discharges through R1, R2, R3 and VR. As C1 discharges, the base voltage of Q1 decreases until its base-emitter junction is forward-biased and is driven to conduction. Q1 then turns on Q2 and the cycle is repeated. If the charging time of C1 is designed to be much less than its discharge time, a pulse signal is generated at the collector of Q1. This pulse signal is used to switch Q3 on and off to generate a sawtooth voltage across C2 at the output.

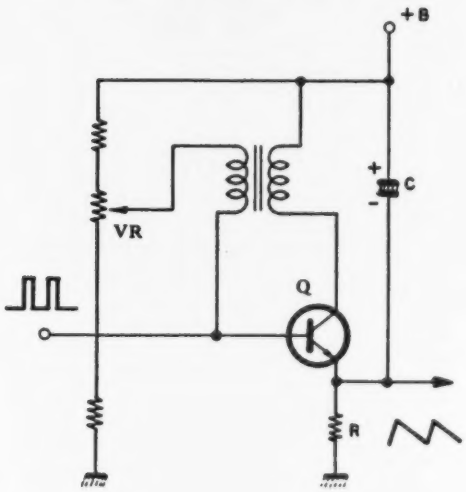
Coupling the sync signal

There are two methods of controlling the frequency and phase of the vertical and the horizontal oscillator circuits. One is by directly controlling the oscillator by injecting the sync signal directly to the circuit. This method is used in the vertical deflection circuit. The other method uses the average of the sync signal to control the horizontal oscillator. This is called sync AFC. This method is used in the horizontal deflection circuit.

Figure 3-24 shows sync signal coupling in a vertical blocking oscillator circuit which uses an NPN transistor. The transistor is turned on by the positive sync signal supplied to the base of the transistor. If an NPN transistor is used, the negative sync signal is used to turn it on.

Without the sync signal applied to the base, the oscillation frequency of the circuit depends largely on the base voltage, as shown in Figure 3-25(a). A lower base voltage yields a lower oscillation frequency; a higher base voltage, a higher oscillation frequency. When the oscillation frequency is set a bit lower than the frequency of the sync signal and the positive sync signal is applied to the base shortly before the emitter voltage or sawtooth voltage reaches its minimum, the pulse triggers the transistor on. This sets the frequency and phase of the sawtooth voltage equal to the frequency and phase of the sync signal. In Figure 3-25(b) the solid sawtooth wave is the output if the sync signal is applied. The dashed wave is the output if the sync signal is not supplied to the base.

Figure 3-24
A sync-signal coupling circuit



Vertical drive circuit

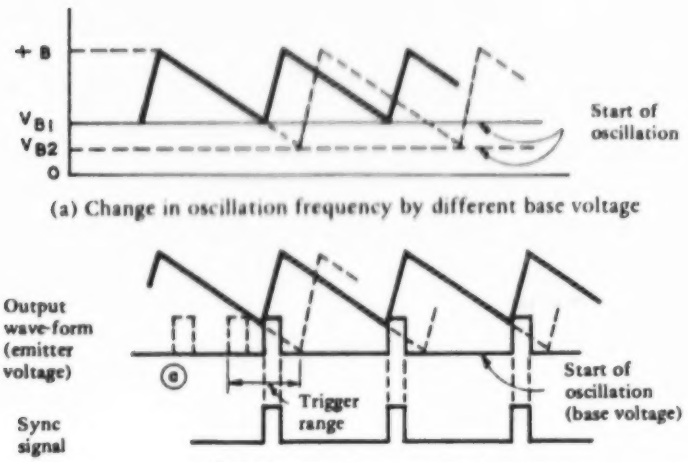
The strength of the sawtooth voltage produced in the vertical oscillator circuit is not enough to drive the vertical output circuit. The vertical drive circuit is used to amplify the voltage enough to drive the vertical output transistors. The vertical drive circuit also improves the linearity of the voltage. The output of the vertical drive circuit should be enough to provide an adequate negative feedback to stabilise the entire vertical deflection circuit. Sufficient output also improves the linearity of the voltage and improves the linearity of the raster.

A common-emitter or an emitter-follower is used in the vertical drive circuit. Figure 3-26 shows a common-emitter drive circuit. VR1 functions as the vertical-size control by varying the amplitude of the sawtooth voltage.

If the sawtooth current flowing through the deflection coil is distorted, the upper or lower part of the raster will either be stretched or compressed. The vertical drive circuit solves this problem by improving the linearity of the current.

Distortion can be caused by: 1) distorted oscillator wave-form, 2) transistor with poor linearity and 3) poor output transformer characteristic.

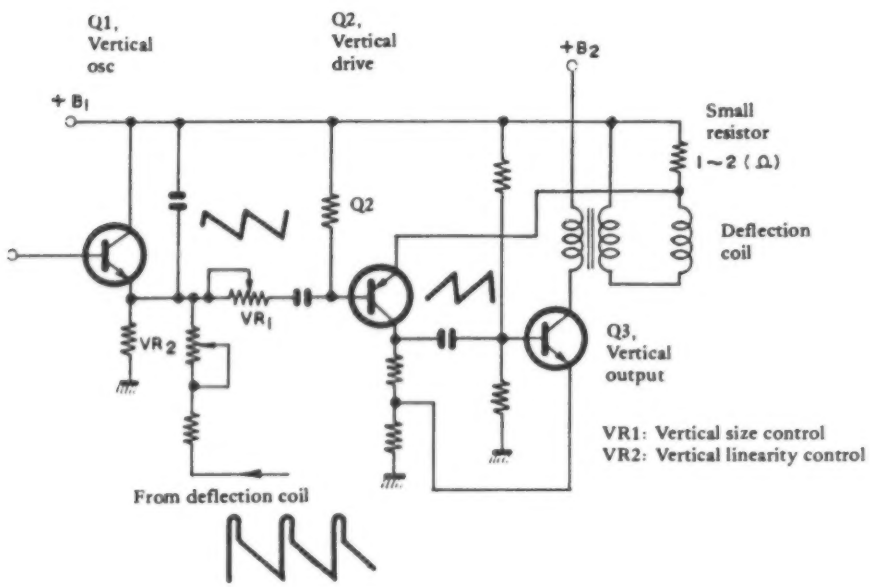
Figure 3-25
Synchronisation of oscillator frequency



(a) Change in oscillation frequency by different base voltage

(b) Triggering by sync signal

Figure 3-26
Common-emitter vertical drive circuit



Many compensation circuits can improve distortion, but poor linearity is mainly improved by negative feedback. Negative feedback is commonly obtained by connecting an emitter resistor to the vertical output circuit. Another method is to allow the deflection coil current to flow through the emitter resistor of the vertical drive transistor.

Special compensation and negative feedback circuits with an integrator are used to improve the oscillator wave-form.

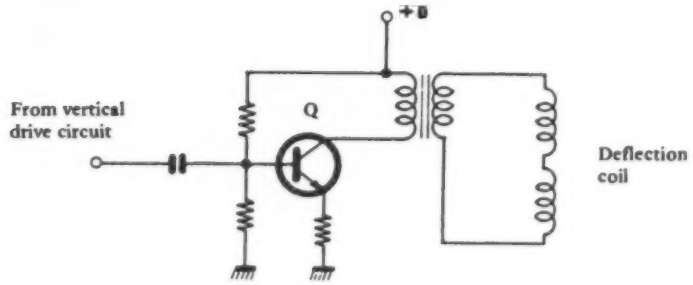
Vertical output circuit

This circuit supplies the sawtooth currents to the deflection coils. The circuits shown in Figures 3-27 and 3-28 are commonly used.

Figure 3-27 shows a common-emitter amplifier circuit. The output transformer is used to couple the circuit to the deflection coil. This circuit is a class-A amplifier with an output power of just a few watts. However, this should be a high-powered transistor because a high-pulse voltage whose strength is several times more than the power supply is generated during the retrace period and coupled to the collector. This high-pulse voltage is generated because of the inductance of the deflection coil. A pulse voltage-limiting circuit is included to limit the magnitude of the pulse voltage generated and to protect the output transistor.

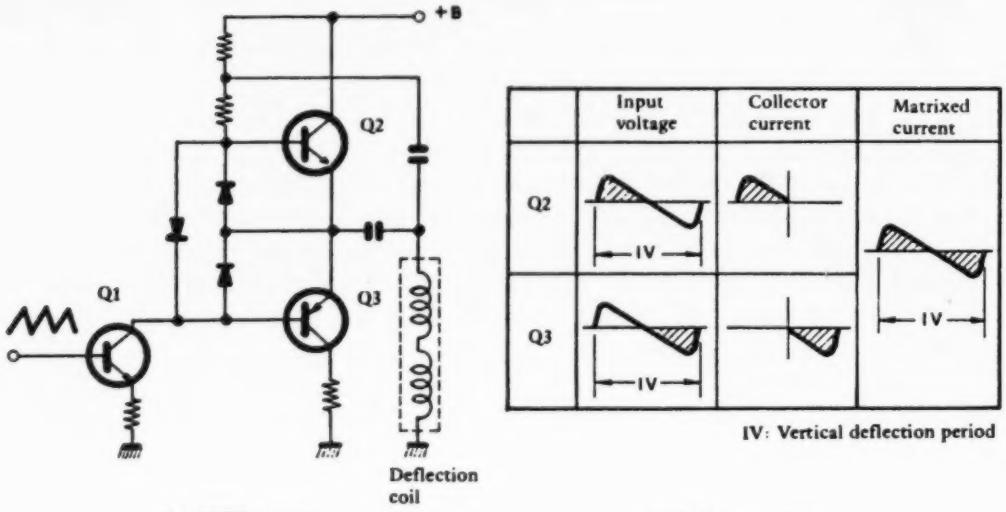
Figure 3-28 shows a single-end push-pull (SEPP) vertical output amplifier circuit. The output transformer is no longer necessary in this circuit. This circuit is commonly used because the linearity of the sawtooth current flowing through the deflection coil is not easily distorted. Q1 is the vertical drive transistor, Q2 and Q3 are the vertical output transistors. The output transistors (NPN and PNP) form a complementary circuit.

Figure 3-27
Common-emitter vertical output circuit



The sawtooth voltage from Q1 is applied to Q2 and Q3. Q2 is on and conducts during the half-cycle of the scanning period, as shown in Figure 3-28(b). After the first half-cycle of the scanning period, Q3 is on and conducts. Both transistors are turned on alternately. The collector currents of both transistors are combined to form the current supplied to the deflection coil to deflect the electron beam vertically. Since the transistors from a push-pull circuit, their characteristics must be the same. The high-pulse voltage generated during the retrace period saturates both transistors. The internal resistance of transistors during saturation is very low. In effect, the transistors function as low resistance parallel to the deflection coil. This lessens the magnitude of the generated pulse voltage, eliminating the need of a protection circuit for the output transistor.

Figure 3-28
SEPP vertical output circuit and its function



(a) SEPP circuit

(b) SEPP operation

Examples of actual vertical deflection circuits

Figures 3-29 and 3-30 show actual vertical deflection circuits. The vertical deflection circuit shown in Figure 3-29 uses a blocking oscillator. A transformer-coupled class-A amplifier circuit is used as an output circuit. The linearity of the sawtooth voltage is improved by the negative feedback from the output and integrator circuit. The thermistor (TH), connected to the base circuit of the output transistor Q3, is used for bias stabilisation. The diode in the collector circuit absorbs the pulses, which are generated during the retrace period. The vertical centre position of the raster is adjusted by the variable resistor marked V-CENT connected to the secondary of the vertical output transformer (VOT). It forms a bridge circuit with the secondary. By adjusting V-CENT, the DC current flow in the deflection coil is varied changing the vertical position of the raster.

The vertical deflection circuit in Figure 3-30 uses a multivibrator circuit as the vertical oscillator circuit. A SEPP complementary circuit is used as the output circuit. This vertical deflection circuit has a dual vertical-drive stage. Q1 functions as a switch in generating a sawtooth voltage. Compensating circuits for the improvement in linearity are omitted due to good response and matching of the SEPP and the deflection coil.

Figure 3-29
A vertical deflection circuit

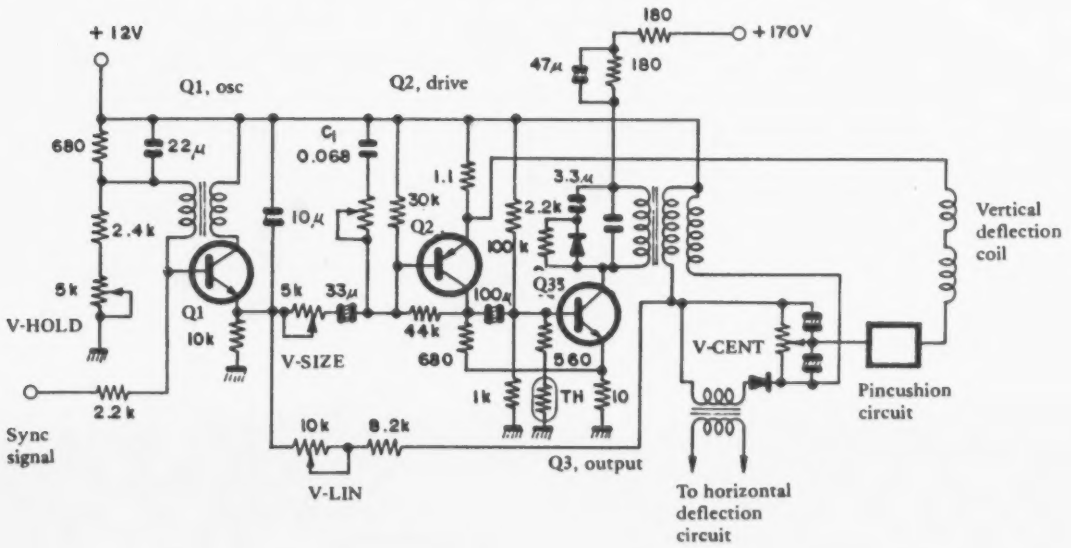
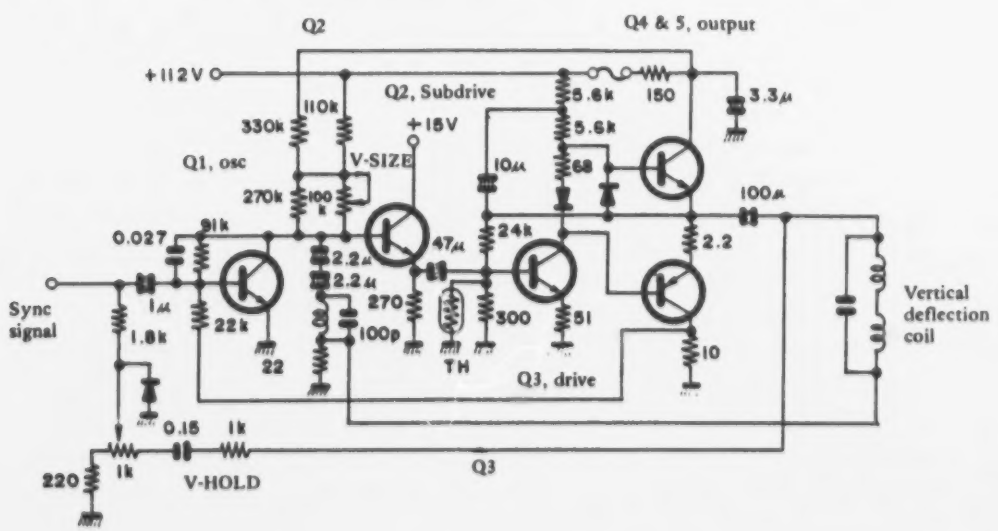


Figure 3-30
A vertical deflection circuit

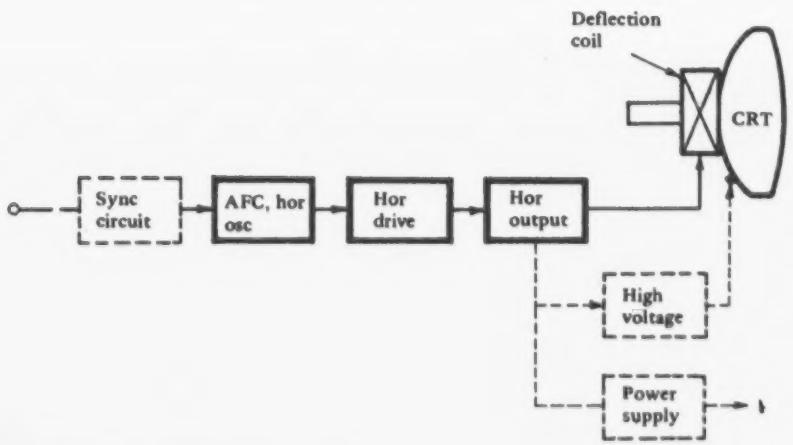


Horizontal deflection circuits (HDCs)

Block diagram of horizontal deflection circuit

The sawtooth current supplied to the horizontal deflection coil has a frequency of 15,750 Hz. Figure 3-31 shows a functional block diagram of the horizontal deflection circuit. It consists of the horizontal oscillator, the horizontal drive and the horizontal output circuits. In addition to these are the AFC, high-voltage generator and power-supply circuits.

Figure 3-31
Functional block diagram of a horizontal deflection circuit



Synchronisation AFC circuit and its function

As mentioned in the section on "Frequency Separator Circuit," the vertical sync signal controls the vertical oscillator frequency. The vertical sync signal is processed by two to three stages of low-pass filter (integrator) circuits that filter horizontal sync signal and noise. The vertical sync signal is then supplied to the vertical oscillator transistor.

On the other hand, the horizontal sync signal is processed by a high-pass filter circuit. Noise between horizontal sync pulses in the TV signal (Figure 3-32) disturbs horizontal synchronisation and causes an unsteady image.

Figure 3-33 shows an example of noise interference in direct horizontal synchronisation. In Figure 3-32, noise lower than the trigger level of the horizontal oscillator will not create interference on the screen. But noise greater than the trigger level of the horizontal oscillator will interfere with horizontal synchronisation and distort the image on the screen. Figure 3-34 shows an image with partial loss in horizontal sync. Noise creates this distortion if the horizontal sync circuits are designed to use each pulse in the horizontal sync signal as a trigger signal to synchronise the horizontal oscillation with the horizontal scanning frequency.

Figure 3-32
Noise between horizontal sync pulses in the TV signal

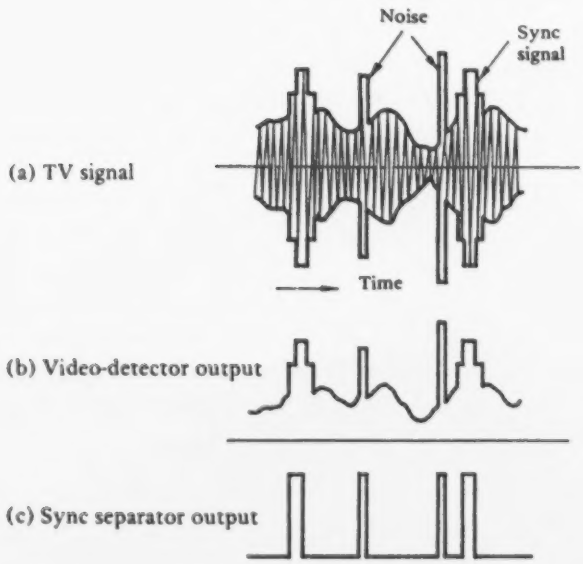
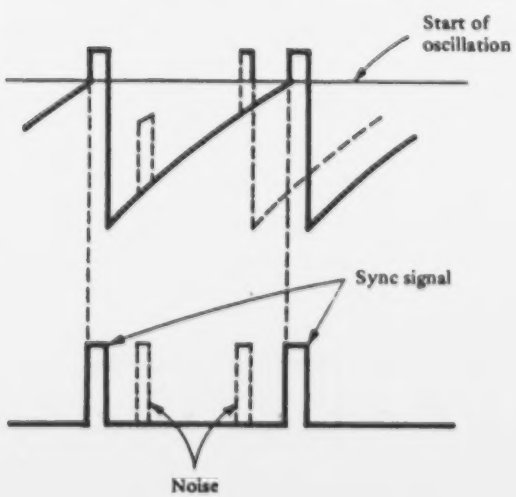


Figure 3-33
An example of noise interference in direct horizontal synchronisation



However, if the sync circuits are designed to respond only to the average of the horizontal sync signal per frame of video information, interference of noise with horizontal synchronisation is minimised. This is because the average of the sync signal is insignificantly affected by the presence of noise. Thus, even continuous noise generated internally by the receiver does not interfere with horizontal synchronisation of the receiver.

The horizontal sync circuit designed to respond to the average of the horizontal sync signal is called the sync AFC circuit. Its functional block diagram is shown in Figure 3-35. It consists of the phase-detector, integrator, horizontal oscillator and comparator signal-generator circuits.

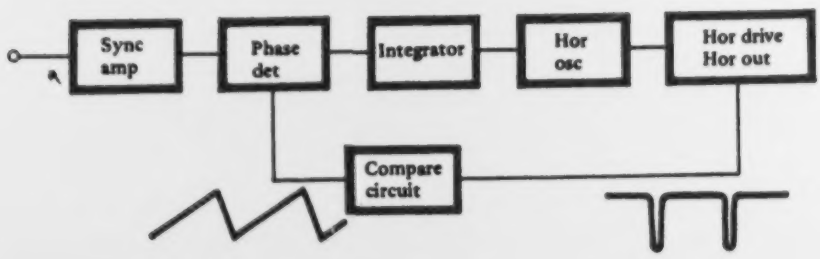
The phase-detector circuit compares the phase of the retrace period of the sawtooth signal (sample signal) with the phase of the horizontal sync signal. When a phase-difference is detected, the detector produces a signal proportional to the difference. This signal is generally a pulse voltage filtered by the integrator circuit before being supplied to the horizontal oscillator circuit as the AFC-control voltage. The control voltage in turn adjusts the phase of the oscillator.

The polarity of the control voltage depends on the phasing of the signals. A positive-control voltage is produced if the phase of the sample signal is faster (higher frequency) than the horizontal sync signal. A special oscillator circuit is designed for the horizontal oscillator, in which its phase and frequency can be controlled by the AFC-control voltage. The sawtooth-wave AFC circuit is commonly used for the horizontal AFC circuit in TV receivers.

Figure 3-34
Partial loss of horizontal synchronisation by external noise

(b) Disturbed reproduction (a) Correct reproduction

Figure 3-35
Functional block diagram of a sync AFC circuit



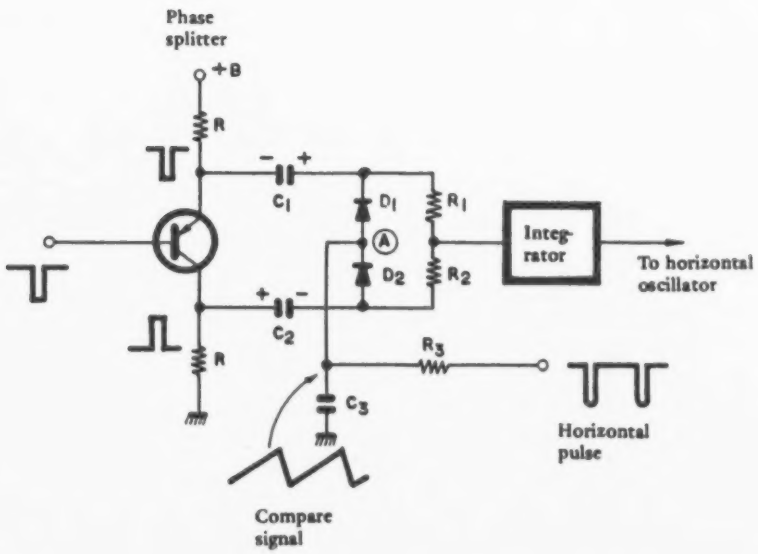
Balanced sawtooth-wave AFC circuit. Figure 3-36 shows a balanced sawtooth-wave AFC circuit. This circuit uses a geometric phase-detector circuit. It requires positive and negative sync signals as reference signals. These signals are

taken from the sync amplifier circuit. The control voltage which varies the horizontal oscillator frequency is produced by the AFC circuit and is generally supplied to the blocking oscillator circuit.

In Figure 3-36, positive and negative sync signals are taken from the collector and emitter circuits, respectively, of the sync amplifier transistor. The horizontal flyback pulses are transformed into a sawtooth signal by the integrator circuit (C3, R3) and supplied to the junction of phase-detector diodes D1 and D2 as a sample signal. The horizontal sync signals are supplied to D1 and D2 as reference signals. The output voltage taken between the junction of R1 and R2 is the control voltage. This voltage is supplied to the base of the horizontal oscillator transistor via an integrator circuit.

The details in the operation of a balanced sawtooth-wave AFC circuit follow.

Figure 3-36
Balanced sawtooth AFC circuit



When the sample signal is not supplied. In Figure 3-37 the magnitudes of the sync signals applied to the phase-detector diodes D1 and D2 are equal. These signals charge C1 and C2 with equal magnitudes but opposite polarities. During intervals between sync pulses, C1 and C2 discharge through R1 and R2. However, since C1 and C2 are charged equally, the voltage at point (B) due to the discharge of the capacitors is zero. Thus the AFC-control voltage is zero.

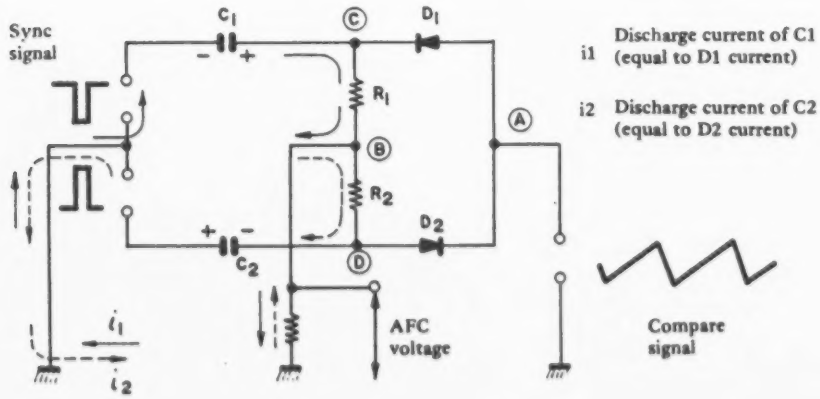
When the sample signal is applied. When the sample signal is applied, the magnitudes of the currents through D1 and D2 depend on the possible phase relations between the horizontal sync signal and the sample signal, as shown in Figure 3-38.

The phase of the sample signal lags behind the sync signal when the

horizontal oscillator frequency decreases as in (a). In this case the sync signals overlap with the sample signal during the beginning of the retrace period, and the signal detected by D1 becomes greater than the signal detected by D2. Thus C1 is charged with a magnitude greater than C2. When they discharge, the AFC-control voltage produced at point (B) in Figure 3-37 is positive.

On the other hand, when the horizontal oscillator frequency increases as in (c), the sync signal overlaps with the sample signal later during the retrace period. In this case the voltage produced at point (B) when the capacitors discharge is negative.

Figure 3-37
Signal process in a phase-detector circuit



The case shown in (c) is the proper phase relation. The signals detected by D1 and D2 are equal, thus producing no control voltage at point (B).

Figure 3-39 shows the relationship of the output voltage of the AFC circuit to the phase difference between the sample and sync signals. The output voltage is integrated (filtered) and supplied to the horizontal oscillator circuit to control the horizontal oscillator frequency.

Unbalanced sawtooth-wave AFC circuit. Figure 3-40 shows an unbalanced sawtooth-wave AFC circuit. Unlike the balanced AFC circuit, it requires only a negative sync signal as reference signal.

Consider first the operation of the circuit when the sync signal is not supplied. When the sample signal is supplied, the diodes conduct alternately. D1 conducts during the positive cycle, D2 during the negative cycle. The direction of the current flow in the circuit during the positive cycle is indicated by the solid curve, while the dashed curve indicates the direction of the current flow during the negative cycle. The currents flowing through D1 and D2 during each half-cycle are equal. C2 is charged alternately by the currents flowing through the diodes. But since the direction of the currents though each diode is opposite, the charged voltage across C2 in a complete cycle is zero.

Consider now the circuit when the sync signal is applied. The sync signal overlaps with the sample signal. Depending on the phase of the sample signal with respect to the sync signal, the current through D1 may be equal to, greater or less than the current through D2. When the oscillator frequency changes, the corresponding control voltage is produced across C2 and then integrated before it is supplied to the horizontal oscillator transistor as an AFC-control voltage.

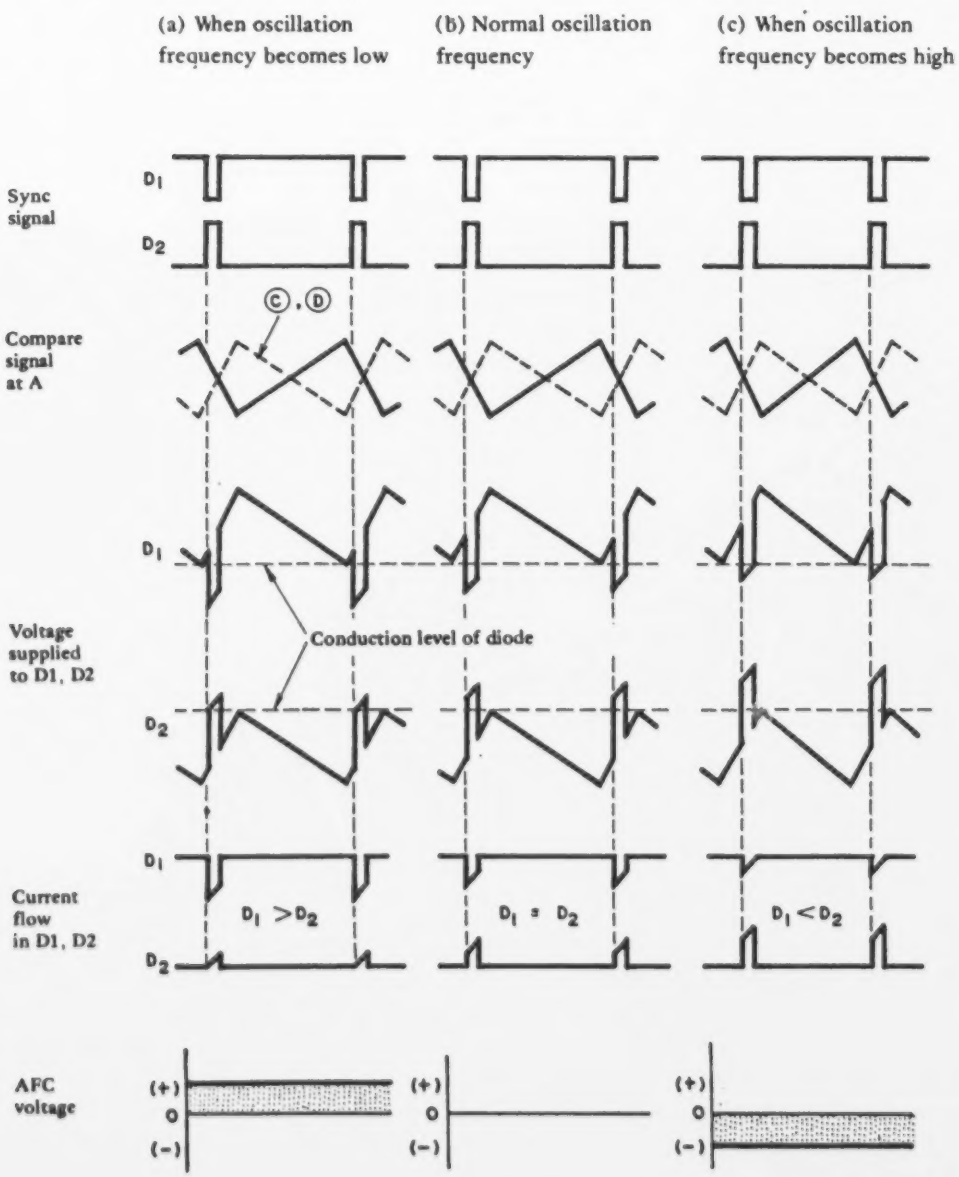


Figure 3-38

Phase relations between horizontal sync signal and sample signal

Figure 3-39
Relationship of AFC output voltage to the phase difference between the sample and sync signals

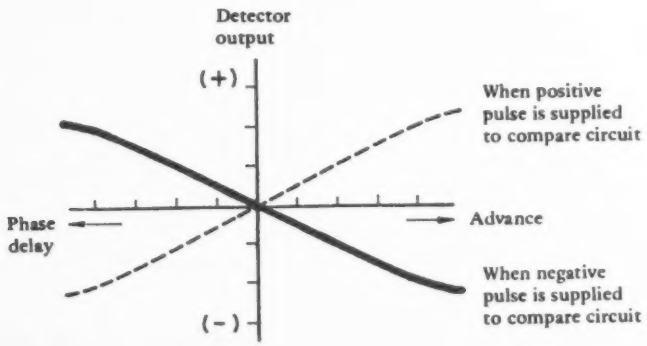
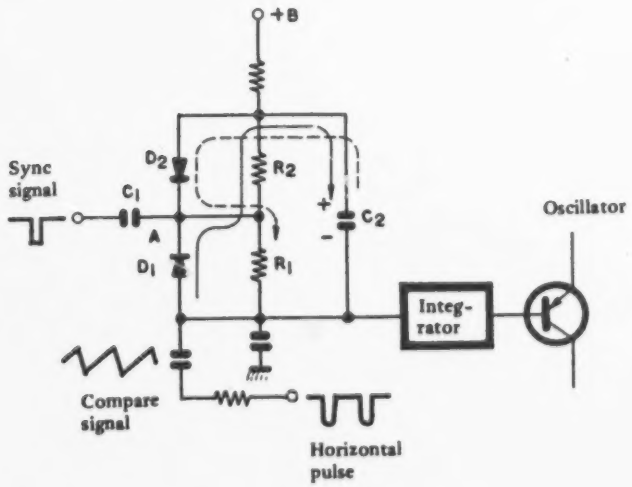


Figure 3-40
Unbalanced sawtooth AFC circuit



Horizontal oscillator circuit

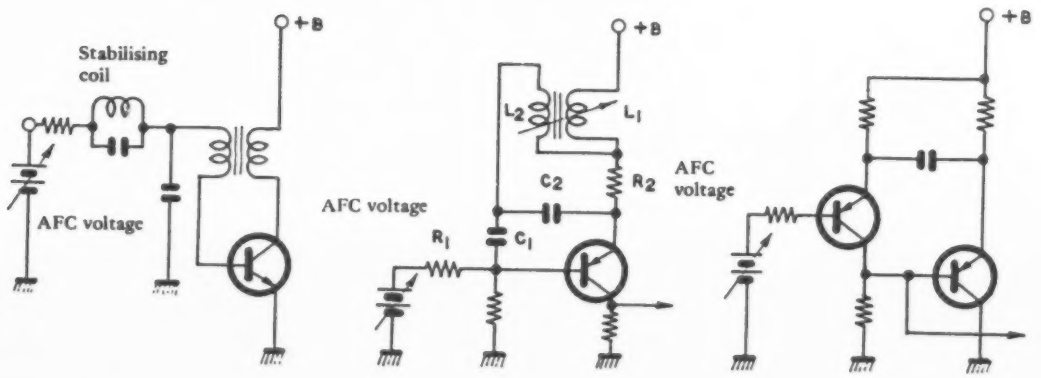
Oscillator circuit. Several types of horizontal oscillator circuits are shown in Figure 3-41. The circuits in (a) and (b) use a blocking oscillator, the circuit in (c) an emitter-coupled multivibrator.

The horizontal oscillator circuit shown in (b) is commonly used because of its simplicity and inherent stability. This circuit combines a blocking oscillator with a Hartley oscillator circuit. L2 and C2 form a resonant circuit with a frequency of 15,750 Hz.

If C2 is removed from the circuit, the base voltage will be a sawtooth wave like the one shown in Figure 3-42(a). If the signal in Figure 3-42(b), which is generated by the resonant circuit formed by L2 and C2 is mixed, the wave in (c) is generated at the base. In (c) the slope of the oscillator at the start of each

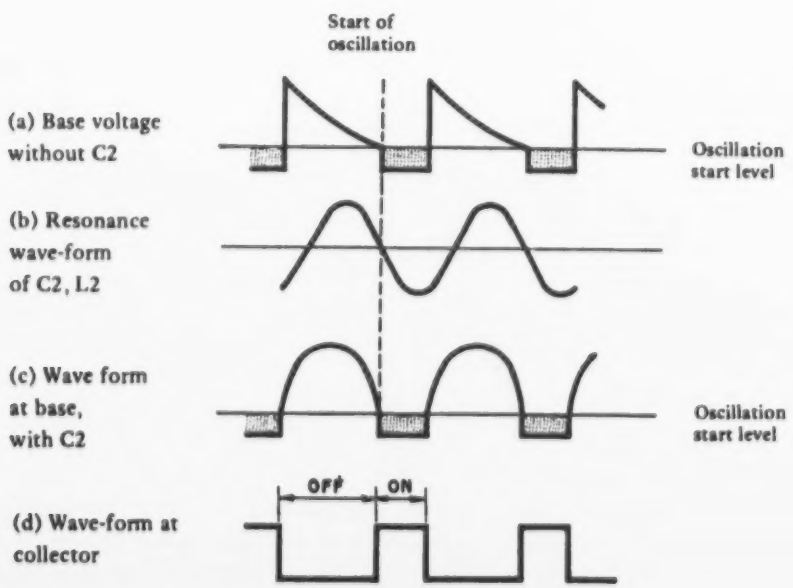
cycle is very steep. The signal is protected from noise interference and the oscillation remains stable even during variations in power supply and temperature.

Figure 3-41
Horizontal oscillator circuit



(a) Blocking oscillator (1) (b) Blocking oscillator (2) (c) Emitter-coupled multivibrator

Figure 3-42
Functional wave-form in the blocking oscillator circuit



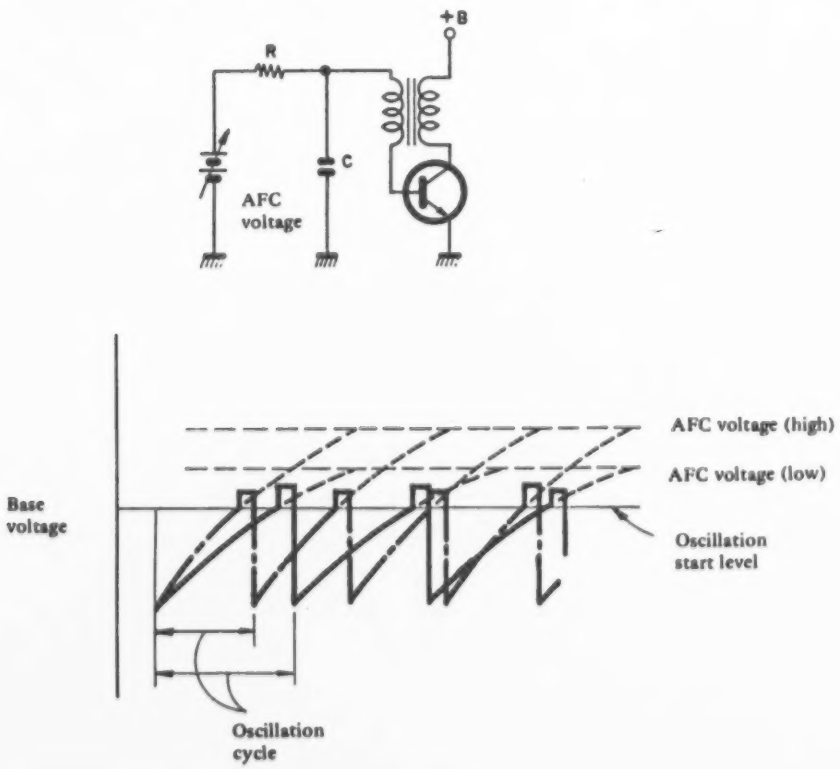
Control of oscillator frequency. The oscillator frequency of the blocking and the multivibrator oscillator circuits depends on the time constant of the circuit and on the supply and base voltages. If the time constant of the circuit

and the supply voltage are fixed (or maintained constant), the oscillator frequency can be varied by the base voltage or the AFC-control voltage. Figure 3-43 shows how the AFC voltage controls the oscillator frequency.

When the AFC voltage is high, C discharges rapidly, resulting in less time between each oscillation. Thus, oscillation frequency is high. When the AFC voltage is low, C discharges gradually, resulting in longer time between each oscillation. Thus, oscillation frequency is low.

Figure 3-44 shows the relationship of the AFC voltage to the oscillator frequency in a circuit where the time constant is fixed. The explanation for a circuit using an NPN transistor is similar but the effects of the AFC voltage on the oscillation are opposite.

Figure 3-43
Oscillator frequency controlled by an AFC voltage



Horizontal drive and output circuit

Horizontal drive circuit. As explained in the following chapter, the horizontal output transistor functions as a mere switch to the horizontal deflection coil. Therefore sufficient base current has to be supplied to the horizontal output transistor so that it can shift from saturation (ON state) to cut-off (OFF state) and vice versa rapidly.

For a supply of sufficient base current, an amplifier is placed between the oscillator and the horizontal output circuit to amplify and improve the output

signal of the oscillator circuit. This amplifier circuit is called the horizontal drive circuit. Figure 3-45 shows a horizontal drive circuit. A transformer-coupled common-emitter amplifier circuit is commonly used.

The horizontal drive transistor operates like the horizontal output transistor. Both transistors operate as a switch. The horizontal output and drive circuits are designed to alternate each transistor as the load of the drive transformer. Thus when the output transistor is ON, the drive transistor is OFF. When the output transistor is OFF, the drive transistor is ON.

Figure 3-44
Relationship between AFC voltage and oscillator frequency

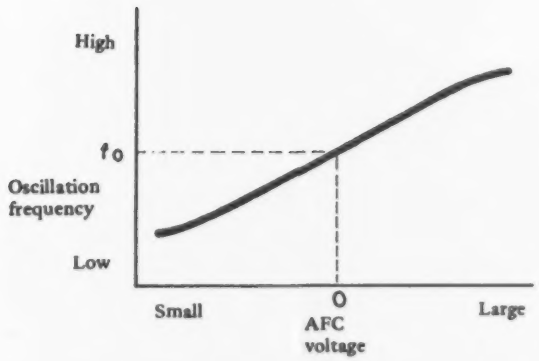
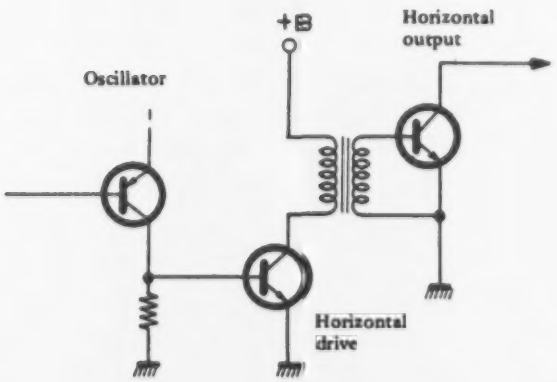


Figure 3-45
Horizontal drive circuit



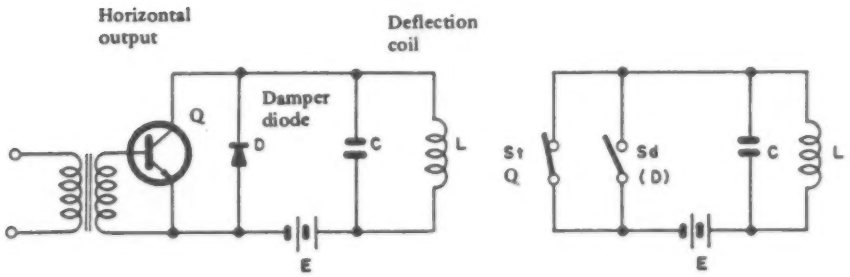
Horizontal output circuit. Figure 3-46(a) shows a horizontal output circuit. The transistor in the circuit is used as a switch. A combination of a transistor and a damper diode produces a sawtooth current for the horizontal deflection coil.

The horizontal output transistor is triggered on by the pulse voltage applied

to its base, and the damper diode conducts whenever the polarity of the stored charge in C supplies a forward-biasing voltage.

Since both the transistor and the damper diode function as a switch, the operation of the circuit can be explained using the equivalent circuit shown in Figure 3-46(b). The horizontal deflection coil can be considered a series connection of its inductance L and its internal resistance r. However, the internal resistance r is so small that the time constant L/r becomes large. Thus a rapidly changing voltage across the coil produces a sawtooth current through it.

Figure 3-46
Horizontal output circuit



(a) Basic circuit (b) Equivalent circuit

Details in the operation of the horizontal output circuit
Figure 3-47 shows a wave-form analysis of the horizontal output circuit.

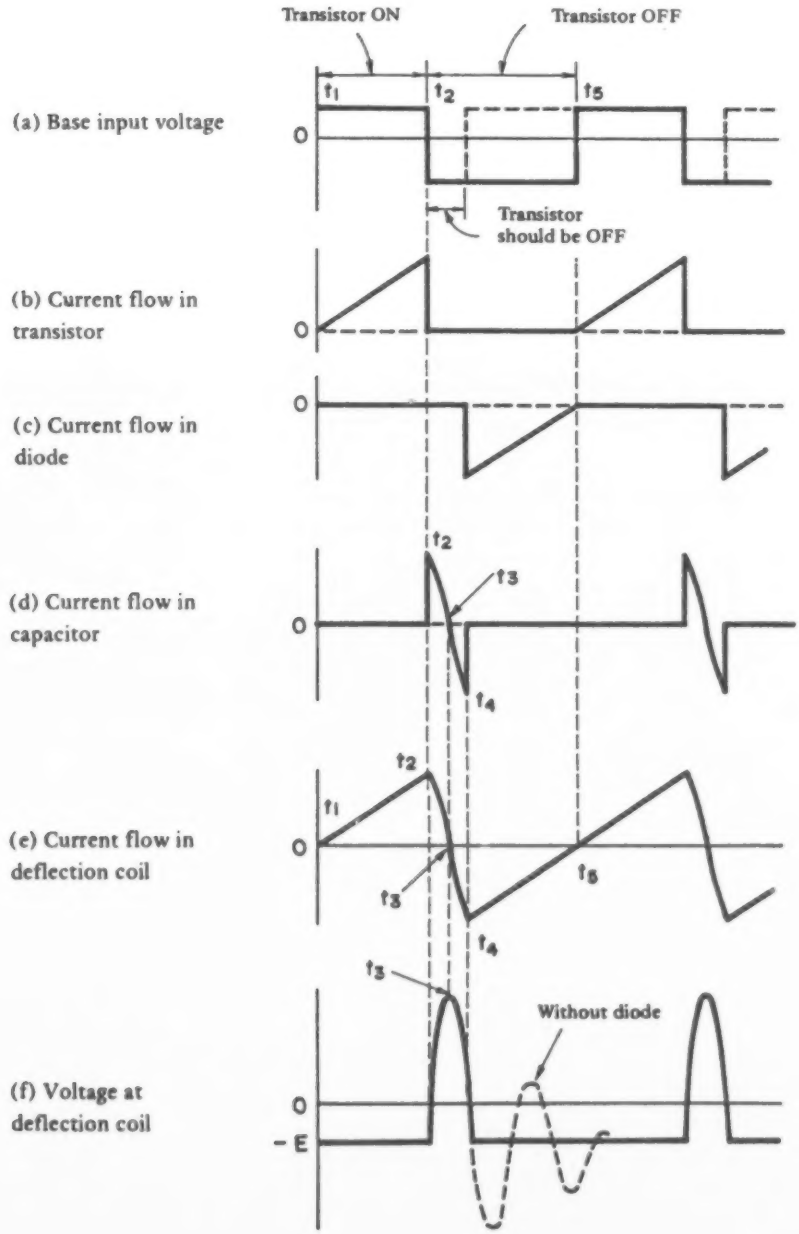
[t1 - t2 period]

When the trigger voltage is applied to the base of the horizontal output transistor, sufficient base current flows and saturates the transistor. The transistor acts as a closed switch St, as shown in the equivalent circuit in Figure 3-46(b). During saturation, the current starts to flow from the power source E to the deflection coil. But the current gradually and linearly increases due to the large time constant of the deflection coil.

[t2 - t3 period]

The horizontal output transistor is driven to cut off by the large negative voltage supplied to the base during this period. The transistor acts like an open switch. The deflection coil and the capacitor C form a resonant circuit. When the current flow through the coil is suddenly stopped by cutting off the transistor, a voltage is induced across the coil. The polarity of the induced voltage is shown in Figure 3-48(d). The induced voltage produces a current flow through C, whose wave-form is shown in Figure 3-47(d). At t3 the current through C becomes zero. At this time C is fully charged and the voltage across it becomes maximum. This maximum voltage is called the flyback pulse voltage.

Figure 3-47
Wave-form analysis of the horizontal output circuit



[t3 - t4 period]

During this period, C discharges through the deflection coil. The current through the coil and C reverses in direction. The current through the coil increases as the stored charge in C decreases. The current becomes maximum at t4 when the voltage across C decreases to zero. Right after C completely discharges, it is charged again. The transfer of energy is only

between L and C, since the damper diode is reverse-biased. Thus the circuit will oscillate at a resonant frequency determined by the values of L and C.

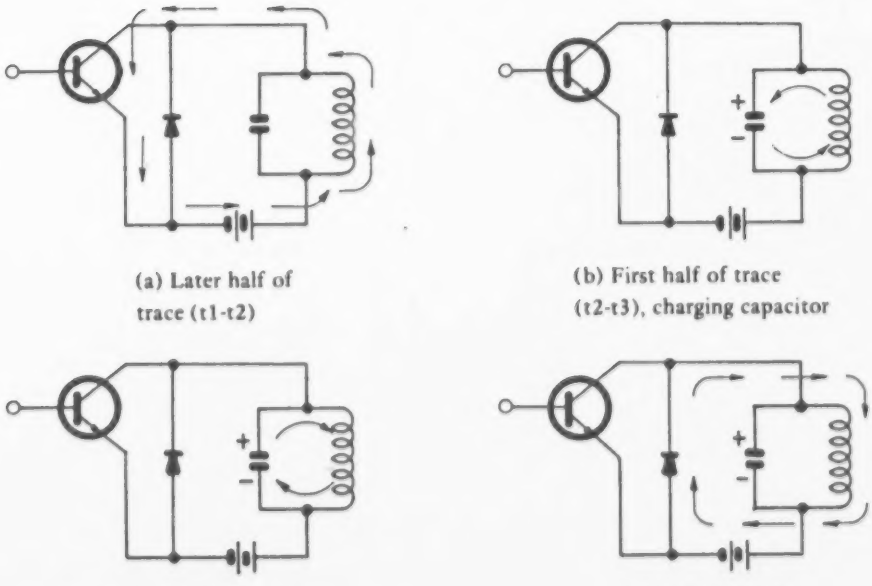
[t4 - t5 period]

At t4 the voltage across C (also across L) is zero and the current flowing through the coil is maximum. This current charges C in a polarity opposing the supply voltage. When the voltage across C exceeds the supply voltage, the damper diode becomes forward-biased. This shorts the LC circuit and stops the oscillation. Because of the long time constant L/r of the coil, the current through the deflection coil does not rapidly decrease to zero. Instead it decreases gradually and linearly until it becomes zero at t5.

Right after t5, a positive triggering voltage is supplied to the base of the transistor and the cycle described above is repeated.

The current flowing through the deflection coil during the trace period is a composite current consisting of the current through the transistor and the damper diode. The wave-form of the current through the deflection coil during the entire cycle is shown in Figure 3-47(e). Figure 3-48 shows the direction of the current flow through the circuit during the entire cycle.

Figure 3-48
Current flow in the deflection coil



(a) Later half of trace (t1-t2)

(b) First half of trace (t2-t3), charging capacitor

(c) Later half of blanking period (t3-t4) discharging capacitor

(d) First half of trace (t4-t5)

Horizontal output transistor and damper diode. A high-powered fast-switching transistor is used in the horizontal output transistor in order to handle the high flyback pulses safely and rapidly shift from saturation to cut-off. A heat sink is attached to the transistor, since heat dissipation is great.

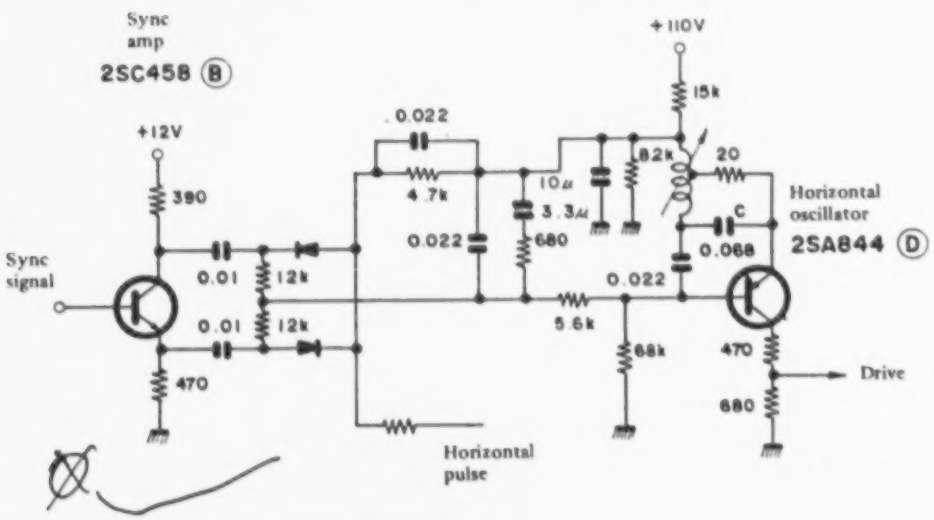
The magnitude of pulse voltage generated during the retrace period is approximately ten times more than the B+ supply voltage. Since the B+ voltage is around 100 volts, the resulting pulse voltage is around 1,000 volts. Thus it requires a transistor with a handling voltage of more than 1,000 volts.

Similar characteristics with less internal resistance are required for the damper diode.

Actual AFC and horizontal oscillator circuit

Figure 3-49 shows a horizontal oscillator circuit. It uses a balanced AFC circuit as its phase detector. The AFC-control voltage is applied to the base of the oscillator transistor. A blocking oscillator circuit is used for the horizontal oscillator. The oscillation frequency is varied by adjusting the core of the horizontal oscillator transformer.

Figure 3-49
An AFC and horizontal oscillator circuit



Actual horizontal drive and output circuit

Figure 3-50 shows a horizontal drive and output circuit. A low-impedance transformer is used to drive the horizontal output transistor. It allows sufficient base current. The coil placed in series at the base circuit of the output transistor will increase the cut-off speed of the collector current.

A pincushion adjustment transformer and linearity improvement capacitor is connected in series to the deflection coil. The function of this circuit is explained in the section on "Pincushion Circuits."

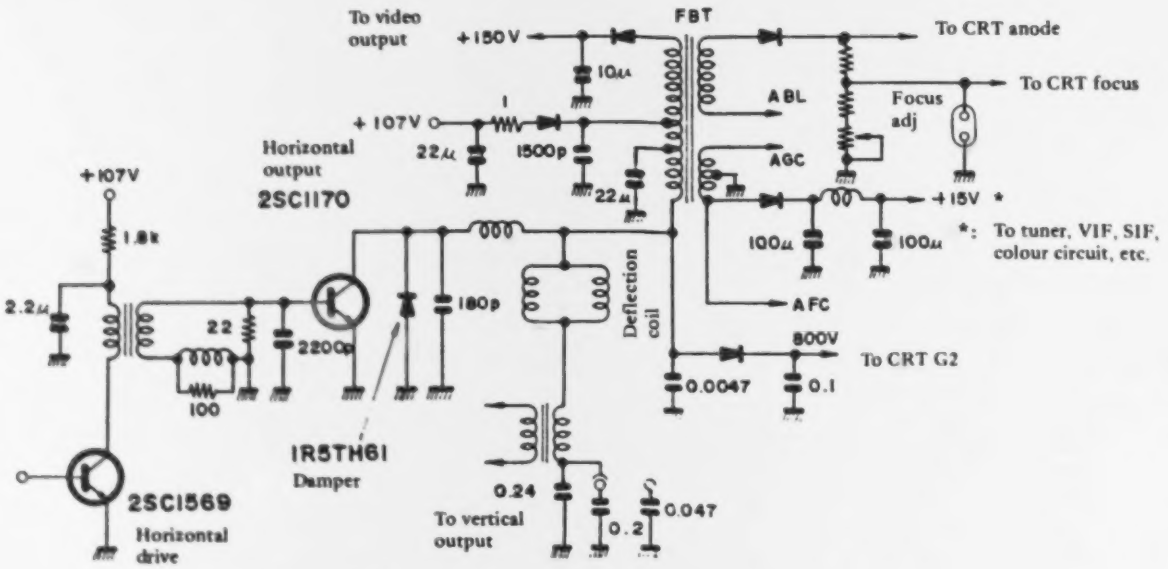


Figure 3-50
A horizontal drive and horizontal output circuit

Surrounding circuits of the horizontal deflection circuits

High-voltage generator circuit

A high voltage of around 25 kV is supplied to the anode of the colour CRT. The high voltage is generated by the horizontal output transformer (HOT) or flyback transformer (FBT), which is connected to the horizontal output transistor, as shown in Figure 3-51. The flyback pulses from the HOT generated during the retrace periods are rectified by the high-voltage rectifier diode and supplied to the anode.

There are three kinds of rectifier circuits: the half-wave rectifier, the voltage doubler and the voltage tripler circuit. The half-wave rectifier circuit is shown in Figure 3-51; the voltage doubler and tripler circuits in Figures 3-52(a) and (b), respectively.

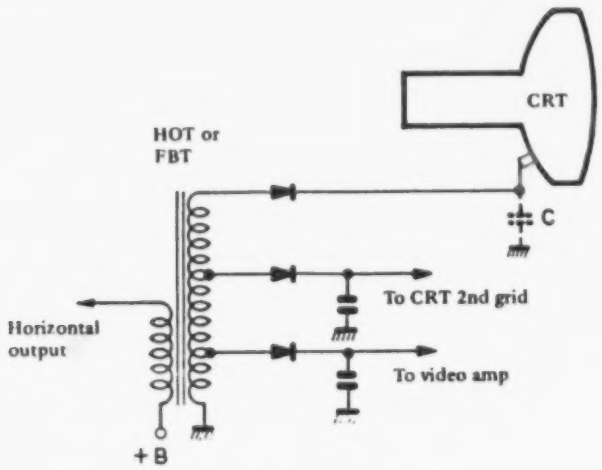


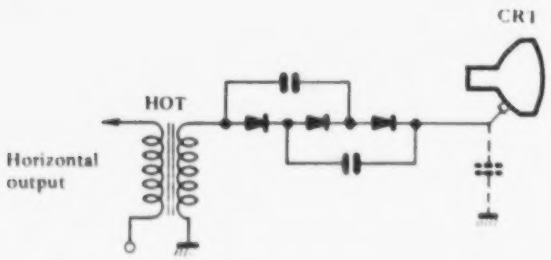
Figure 3-51
High-voltage generator circuit (half-wave rectifier)

The magnitude of the flyback pulses generated during the retrace period is around 1 KV. If the half-wave rectifier circuit is used, the winding ratio of the HOT must be high; thus the transformer becomes big. But if the voltage doubler or tripler circuit is used, the winding ratio and the size of the HOT can be made smaller.

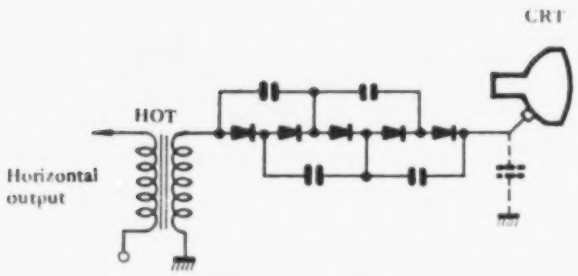
Figure 3-53(a) shows the principle of the voltage doubler circuit. When the pulse voltage e1 [Figure 3-53(b)] is applied, C1 is charged up to the level of e1 by the current flow indicated by the dashed curve (1). When e2 is applied, D2 conducts and capacitor C2 is charged by the current flow indicated by the dashed curve (2). C2 is charged by e2 plus the voltage stored across C1, which is e1. Thus the voltage charged across C2 is equal to e1 + e2. When another positive pulse e1 is applied again to the circuit, D3 conducts and the voltage (e1 + e2) + e1 = 2e1 + e2 appears across C3. This circuit originally works as a voltage tripler circuit for a sine wave input. However, since the level of e2 is much smaller

than e1, the circuit is considered a voltage doubler rectifier circuit.

Figure 3-52(b) shows a voltage tripler rectifier circuit. The circuit is actually a doubler circuit with an additional set of rectifier circuits. If the input to the circuit is a sine-wave, the output becomes five times that of the original voltage.



(a) Voltage doubler



(b) Voltage tripler

Figure 3-52
High-voltage generator circuits

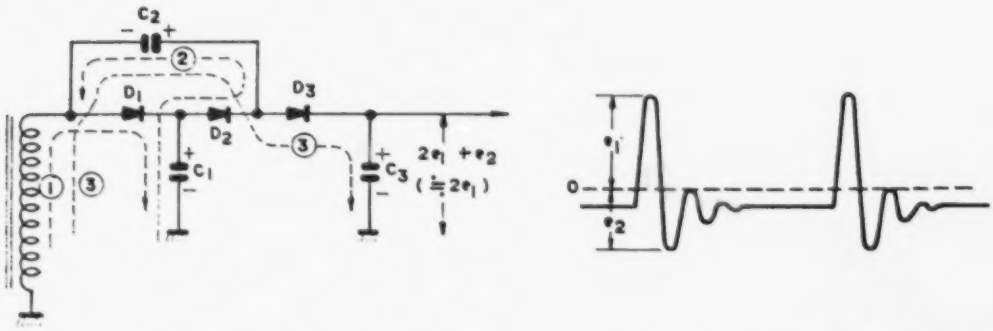
High-voltage stabilisation

Owing to a large beam current value and the reproduction of DC components of the image in colour CRT circuits, the average of the beam current value in the colour CRT varies considerably as the image on the screen changes. The HV of the colour CRT is generated by the flyback pulses. This voltage generation, however, has poor regulation which causes changes in the size of the raster, poor convergence, poor focus, and affects the function of other circuits using the flyback pulses as a power-supply voltage.

Figure 3-54(a) shows a high-voltage stabilising circuit. This circuit does not use any particular control circuit, but the HOT is tuned to the harmonics of the flyback pulses.

The HOT is tuned to the third and fifth harmonics. If the HOT is tuned to the fifth harmonics, the peak of the pulse at its secondary is wider, as shown

in Figure 3-54(a). Therefore the conduction angle of the rectifier becomes wider and the stability of the high-voltage supply is improved.



(a) Basic circuit (b) Wave-form at HOT

Figure 3-53
Voltage doubler in a high-voltage circuit

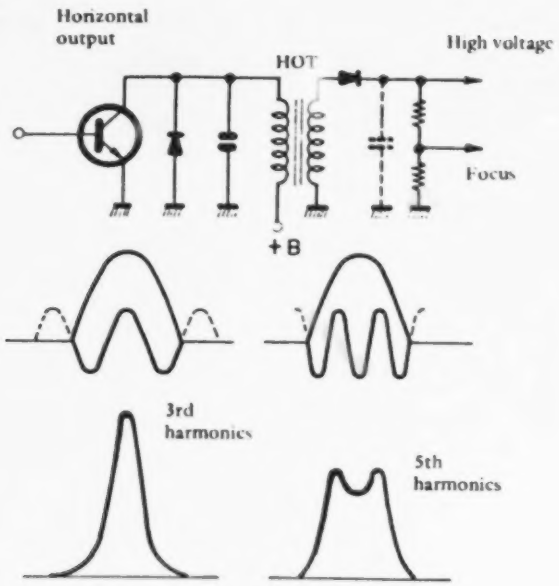
Focus circuit

There are two kinds of focus circuits commonly used in colour CRT circuits. They are the low-voltage static focusing circuit (LV type) and the high-voltage static focusing circuit (HV type). The LV type is usually used for small colour CRTs (less than 20 inches) where the screen grid voltage is used for the focus voltage of the CRT.

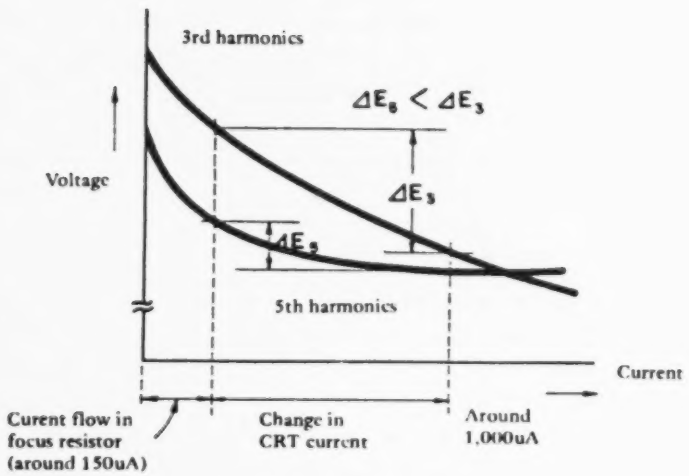
In the HV type the focus voltage is around 16 per cent to 20 per cent of the anode voltage. The focus voltage must be able to follow the change in the anode voltage as fast as possible. Figure 3-55 shows a focus circuit.

Medium- and low-voltage power-supply circuit

Various kinds of power-supply circuits are connected to the HOT circuit,as shown in Figure 3-56. The type of circuits connected varies with its corresponding load. For instance, for a load like the CRT screen which requires a considerably high voltage but a small current, flyback pulses are used. And for a load like the filament of the CRT which requires a low voltage but a high current supply, the supply is taken from the secondary of the HOT. The secondary winding of the HOT generates reverse polarity pulses during the trade or scanning period. These pulses are rectified and used for the filament voltage and for circuits requiring low-voltage supply. Since these rectified pulses are wide, they are not significantly affected by the change in the high and AC voltage and thus provide a relatively stable low-voltage supply.



(a) Wave-form at secondary of horizontal output transformer



(b) High-voltage stabilisation

Figure 3-54
High-voltage stabilising circuit

Figure 3-55
A focus circuit

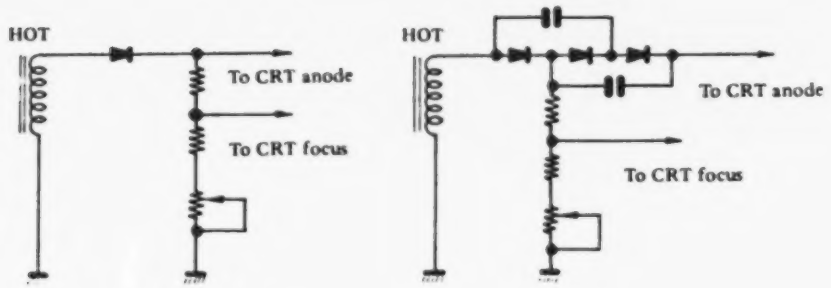
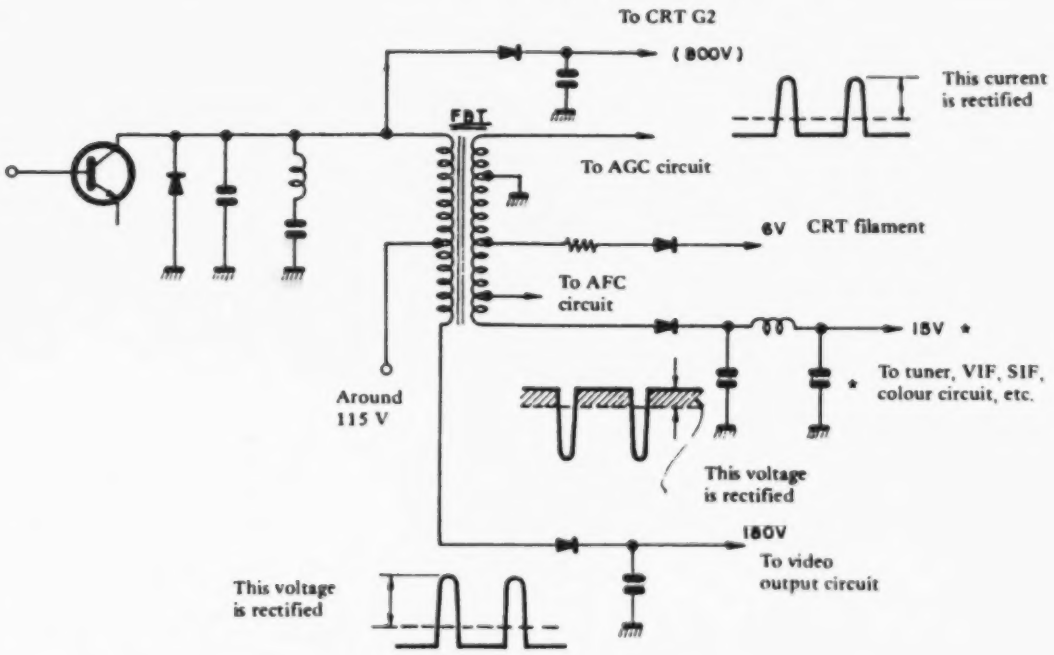


Figure 3-56
Medium and low-voltage power-supply circuit



Pincushion circuits

The screen of the CRT is a curved surface which is not symmetrical to the deflection centre. The distance between the deflection centre and the screen is greater at the corners of the screen. As the beam is deflected linearly towards the corners of the screen, the distance it travels from the gun to the screen increases. This results in the beam's being deflected more at the corners. Thus a spool-shaped raster is produced. This distortion, called pincushion distortion, is greater in wide-deflection angle CRTs.

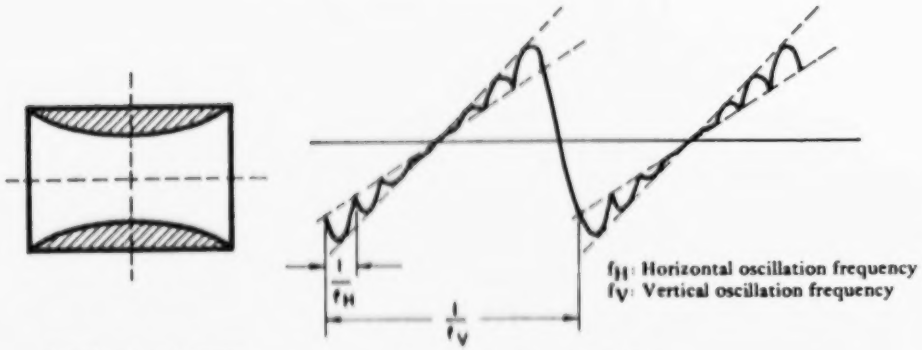
To compensate for the distortion of the raster, the current through the deflection coils must be controlled as the beam is deflected. This is done by the pincushion-control circuit of the horizontal and vertical deflection circuits.

Vertical pincusbion circuit

In Figure 3-57(a) the vertical pincushion distortion can be attributed to insufficient deflection at the upper and lower edges of the screen. To eliminate the distortion, a tolerance or compensating current has to be supplied to the vertical deflection coil. Because of the physical structure of the CRT, the distortion at the edges is parabolic. This parabolic distortion is compensated by adding a parabolic current to the vertical deflection current, as shown in (b). The frequency of the compensating current should be equal to and in phase with the horizontal deflection current. Furthermore, the amplitude of the parabolic current should be greater when the beam is deflected at the upper and lower edges of the screen.

A saturation reactor in Figure 3-58(b) is used to generate the parabolic current. Figure 3-58(a) shows a typical vertical pincushion circuit. For CRTs with a deflection angle of less than 90 degrees, the vertical pincushion distortion is minimal. Thus, instead of using a pincushion tolerance circuit, the winding of the vertical deflection coil is designed to compensate the vertical pincushion distortion.

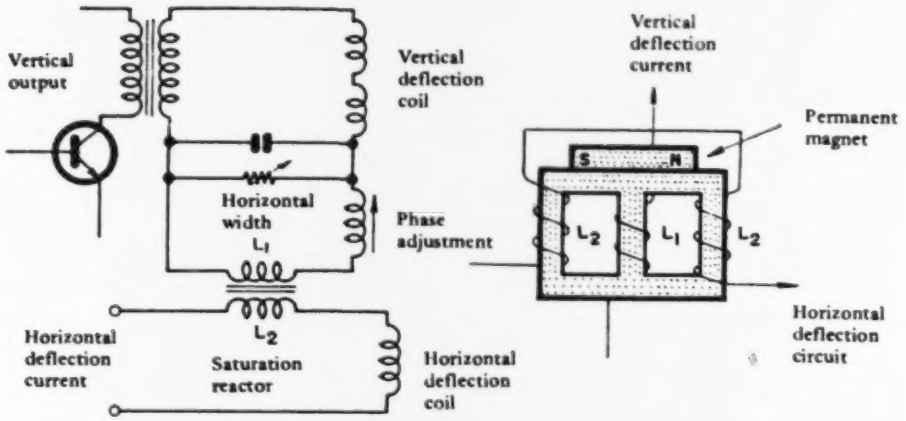
Figure 3-57
Compensation of upper and lower pincushion distortion



(a) Upper and lower pincushion distortion

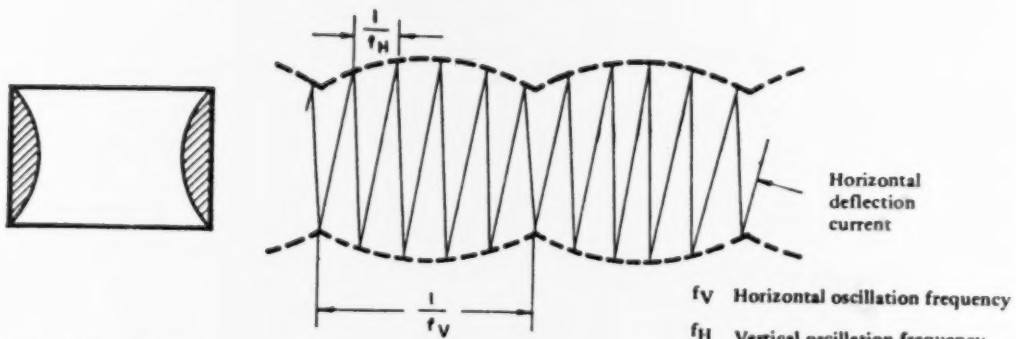
(b) Current needed for compensation

Figure 3-58
Compensation circuit for upper and lower pincushion distortion



(a) Compensation circuit (b) Saturation reactor

Figure 3-59
Compensation of right and left pincushion distortion



(a) Right and left pincushion distortion

(b) Compensation current

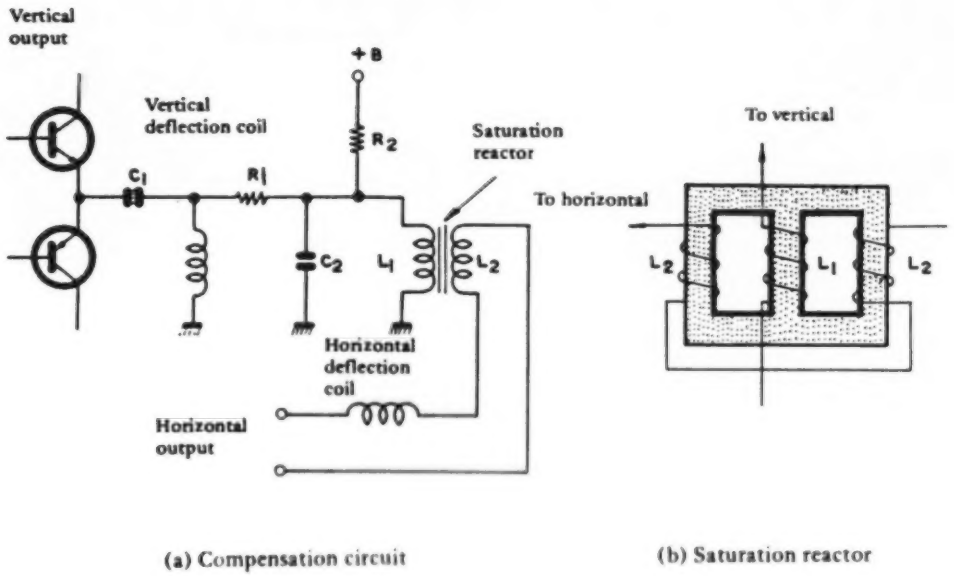
Horizontal pincushion circuit

Figure 3-59(a) shows a horizontal pincushion distortion which can be attributed to insufficient deflection at both sides of the screen. This distortion is eliminated by modulating the horizontal deflection current with a compensating current. A parabolic current with a frequency and phase equal to the vertical deflection current is used to modulate the amplitude of the horizontal deflection current. The resulting horizontal deflection current is shown in (b).

The circuit in Figure 3-60(a) is used to generate the compensating current.

It uses a saturation reactor, shown in (b). The inductance of the reactor decreases when the compensating current (through L1) increases and it increases when the compensating current decreases. The parabolic current from the integrator circuit formed by R1 and C2 is supplied to L1. This produces a parabolically amplitude-modulated horizontal current through the horizontal deflection coil, which eliminates the horizontal pincushion distortion.

Figure 3-60
Compensation circuit for right and left pincushion distortion



(a) Compensation circuit

(b) Saturation reactor

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